Tabriz Journal of Electrical Engineering (TJEE), vol. 55, no. 1, 2025 Serial no. 111
DOI: 10.22034/tjee.2024.61133.4827

Bi-Potential Diagram Method for Designing of a Single-Electron AND Gate

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Received: 07/04/2024, Revised:16/06/2024, Accepted: 01/08/2024.

Abstract
In this paper, bi-potential diagram method which can describe the physical behavior of single electron devices (SEDs) is introduced. Moreover, this technique is used to design a single electron AND (SEA) gate. Besides, the time analysis of the proposed SEA is discussed. Additionally, the principles of bi-potential diagram method are explained, and the associated point of view is described. It is demonstrated that bi-potential diagram is able to explain coulomb blockade phenomenon and time analysis of SEDs. Furthermore, it provides the ability to design and to optimize SEDs effortlessly. The results are confirmed by SIMON software, and the advantages of the introduced approach are shown.

Keywords
Single-electron, AND gate, Coulomb blockade, SIMON.

1. Introduction

Single-electron devices (SEDs) are nanoscale electronic systems which provide the ability to control precisely small amounts of charge (a single electron). In these devices, the dimensions are small so that they let electrons to move only one-by-one. This leads to new coulomb characteristics which are observed exclusively in this field of study. SEDs are very small with ultra-low power consumption; therefore, they are of interest in electronics [1]. Subsequently, according to the progress in lithography, they may be likely candidates for replacing MOSFETs in the future. SEDs have been used in many designs as digital gates [1 and 2]. Their structure generally consists of islands, tunnel junctions, and capacitors. An island is a very small piece of conductor or semi-conductor in nanometer dimensions and is placed on an insulating medium, and is in contact with the surrounding environment only through tunnel or capacitive connections. The sum of the tunneling resistances of each island with its surrounding environment should be large enough so that the electron can be replaced in the island. Considering this condition with the limit of quantum uncertainty gives the minimum value of the sum of the mentioned resistances (R_T) as [3]:

$$R_T \gg \frac{h}{e^2} = R_Q = 25813\Omega \quad (1)$$

where h is Planck's constant, e is the elementary charge, and R_Q is the quantum resistance. Nowadays, SEDs are still limited to low temperatures; however, the research on them continues seriously [4].

So far, various digital gates have been designed based on single-electron components [4-8].Moreover, we have the experience of introducing logic gates by other technologies [9]. In this paper, we introduce the bi-potential diagram method to design a single-electron AND (SEA) gate, and show the benefits of this technique. The conventional method that is used to analyze SEDs is based on the calculation of transition rates and solving the governing (master) equation [5-8 and 10-13]. This calculation method does not provide any physical view of the mechanism of SED's performance, and includes very complicated computations. The mentioned issues deny the possibility of optimization and even design in many cases. On the contrary, the bi-potential diagram not only explains the physics of electron transfer in SEDs, but also provides the time behavior and the possibility of optimal design.

Subsequently, in section 2, the physical structure and equivalent circuit of the designed SEA are presented, then the general principles of bi-potential method are explained. Consequently, it is used to design the introduced SEA, and the time behavior is modeled. In section 3, the simulation results via SIMON software are proposed. Finally, the conclusion is done in section 4.

2. Materials and methods

In this section, a brief overview about the fabrication process of the SEA gate is put forward. Afterwards, the equivalent circuit is presented, as well as the expected logic performance is described. Subsequently, the principles of the bi-potential diagram method are explained, and it is employed to design the SEA.

2.1. SEA gate structure

According to Fig. 1, photoresist is applied on a prepared metal-layered SiO_2 wafer, then e-beam is used to open the required windows using mask. Next, acid is hired to remove the extra sections so that islands and tunneling junctions are produced. Fig. 2 illustrates the physical structure of the SEA gate which has an island, three tunnel junctions, and one capacitive junction. The

capacitive junction is connected to the voltage of Vg as regulator, and no current can pass through it.

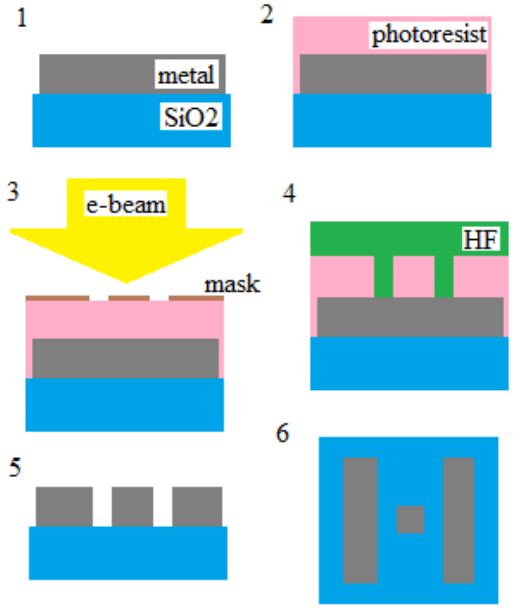

Fig. 1. The suggested fabrication process for SEDs.

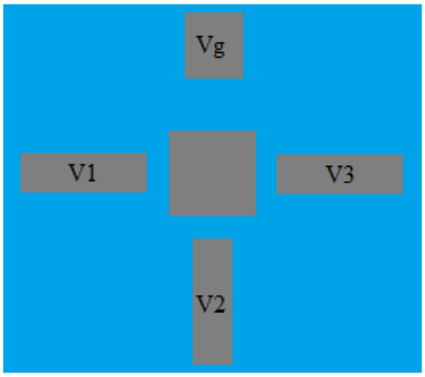

Fig. 2. Up view of the designed SEA.

The voltages of V1 and V2 play the role of input for SEA gate, and the average current of the voltage V3 is assumed as the output of gate. The values of the mentioned voltages should be designed so that the gate operates appropriately. The circuit model used for single electron components is based on island junction capacitors and resistors, as demonstrated in Fig. 3. The voltage of island is V_i.

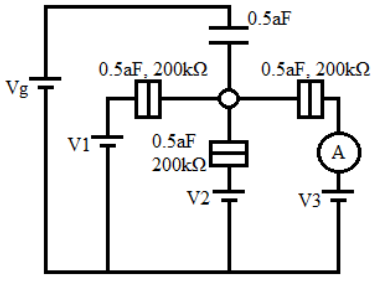

Fig. 3. The equivalent circuit of the introduced SEA.

The truth table of SEA gate is shown in Table I, and the associated time performance is illustrated in Fig. 4. According to Fig. 4, it is expected so that the average current passing through tunnel junction of 3 is being increased when input state is 11.

Table I. The truth table of the designed SEA gate.

Input State (V_1V_2)	Output State (Average of I_3)
00	0
01	0
10	0
11	1

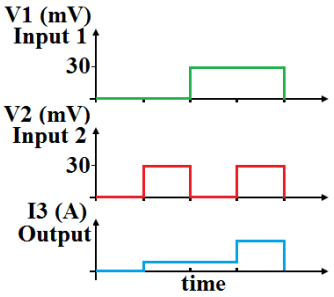

Fig. 4. The expected operation of the proposed SEA.

2.2. Bi-potential diagram

The bi-potential diagram method is based on the physical fact that there are two potential levels to describe the function of electrons. For instance, consider an electron that is placed inside an island, while there is no other electron in this environment. In this case, this electron does not feel its own voltage; therefore, it can move to any point of island. However, the surrounding electrons (in junctions) feel the voltage of island's electron. Consequently, a potential difference can be defined for the movement of electrons from the contact to the island, and another potential exists in the movement from the island to the contact. This fact is due to the small dimensions of the islands, because the amount of total capacitor connected to the island is low in small dimensions. The difference between the two mentioned potentials is modeled as:

$$V_d = \frac{e}{C_T} \tag{2}$$

In (2), C_T is the total capacitance connected to the island, and V_d indicates the difference in voltage levels. In fact, V_d corresponds to the voltage level that the electrons around the island see the electrons inside the island in it. Next, to employ the bi-potential diagram method, firstly the island's voltage is calculated through the equivalent circuit, where this voltage reveals the state of equilibrium. Then for each island a cylinder is considered where the electrons are shown as ellipses inside it. For each tunneling junction, a line next to relevant island is used. These lines propose the energy level of tunneling contacts associated to their voltages. For example, Fig. 5 displays an island with two tunneling junctions of 1 and 2 with energy levels of E1 and E2, respectively. Here, Ei is the energy level of island, related to island voltage, calculated by equivalent circuit. Ed is related to V_d , (2).

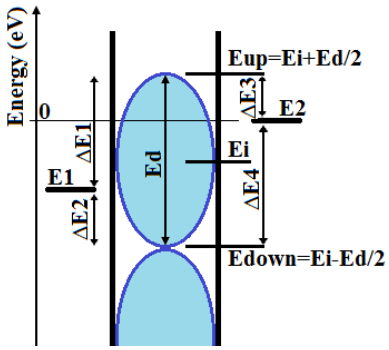

Fig. 5. Bi-potential diagram of an island with two tunneling junctions.

In Fig. 5, when an electron wants to move from contact 1 to the island, it encounters an energy difference of ΔE1. Assuming absolute zero temperature (0 ºK/-273.15 ºC) condition, it can be stated that this transfer will not happen, as Eup is higher than E1. Also, during movement from the island to contact 1, the electron will face the energy barrier of ΔE2, where this movement is not possible (Edown is lower than E1). Similarly, the values of ΔE3 and ΔE4 are employed to discuss electron transfer between contact 2 and island. This system will be in a coulomb blockade state (at absolute zero temperature), despite the fact that there is difference between the contact voltages and island voltage. Here, the power of the bi-potential diagram is absolutely obvious, where it simply provides physical view of carrier transportation and why coulomb blockade happens. Moreover, it allows a simple analysis, and gives direction to the designers.

In general, the steps of bi-potential diagram method are simply as:

1. Calculate difference voltage (V_d) and island voltage (V_i) using equivalent circuit.
2. Draw energy diagram based on V_d, V_i, and contact voltages.
3. Investigate energy levels and possible transferring paths.

2.3. Calculations of bi-potential diagram for the SEA

When input state is 00 (V1=V2=0 V), the output is expected to be 0 (<I3>= 0A), where coulomb blockade happens. As one of the contacts is raised to 30 mV (state 01: V1=0, V2=30 mV, state 10: V1=30 mV, V2=0), some electrons may be tunneled to the island from junction 3 due to the probability nature of electron transformation. However, in the case the amount of output (<I3>) should not be significant. In state 11 (V1= 30 mV, V2=30 mV), bi-potential diagram should be modified so that the change of energy levels lets the electrons to jump from V3 to island. Therefore, the output (<I3>) is increased notably and the output state gets 1. According to the equivalent circuit in Fig. 3, the calculated V_d value is equal to:

$$V_d = \frac{e}{C_T} = \frac{1.6\times10^{-19}}{2\times10^{-18}} = 80mV \quad (3)$$

This means that each electron in the island leads to an energy deference of Ed=80 meV. Also, in this design, the voltage values of contact 3 and gate capacitor connection are equal to:

$$V_g = -115mV, V_3 = 10mV \quad (4)$$

The temperature is considered to be 0 ºK. Next, the island voltage for various states are compute as:

State 00: In this state, the V1=V2=0 V, the island voltage is:

$$V_i = \frac{10mV\times0.5aF}{2aF} - \frac{115mV\times0.5aF}{2aF} = -26.25mV \quad (5)$$

According to Fig. 6(a), the bi-potential diagram in this case shows that coulomb blockade is taken place, and no current exits in the output (I3=0 A).

State 01/10: Considering V1=0 V and V2=30 mV, for the island voltage we have:

$$V_i = \frac{30mV\times0.5aF}{2aF} + \frac{10mV\times0.5aF}{2aF} - \frac{115mV\times0.5aF}{2aF} = -18.75mV \quad (6)$$

According to Fig. 6(b), the bi-potential diagram in this case shows that it is possible to have a low amount of jumping electrons to V2, and when the island gets empty an small current of I3≠0 A exists in the output of SEA gate.

State 11: The input voltages of these states are V1=V2=30 mv, and the calculated island voltage is:

$$V_i = \frac{2\times30mV\times0.5aF}{2aF} + \frac{10mV\times0.5aF}{2aF} - \frac{115mV\times0.5aF}{2aF} = -11.25mV \quad (7)$$

Fig. 6(c) shows that the bi-potential diagram of this case shows that both voltage levels of V1 and V2 are in a position which island electron can tunnel to them. Afterwards, the island gets empty and the electrons of V3 (located at energy level of E3=-10 meV) see that the energy level of island is in a lower amount (Edn=-28.75 meV). Subsequently, the probability of tunneling to the island increases, and the output (I3) rises to the state of 1.

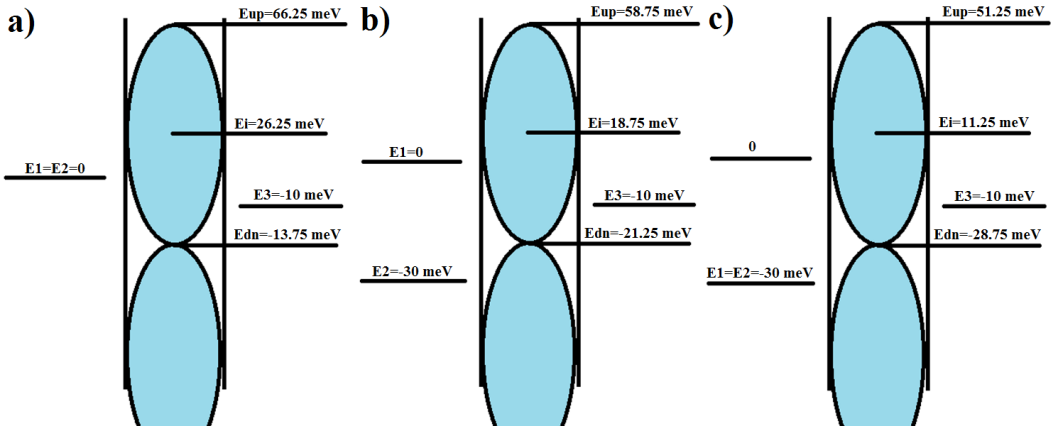

Fig. 6. Bi-potential diagram of the presented SEA for input states of: a) 00, b) 01/10, and c) 11.

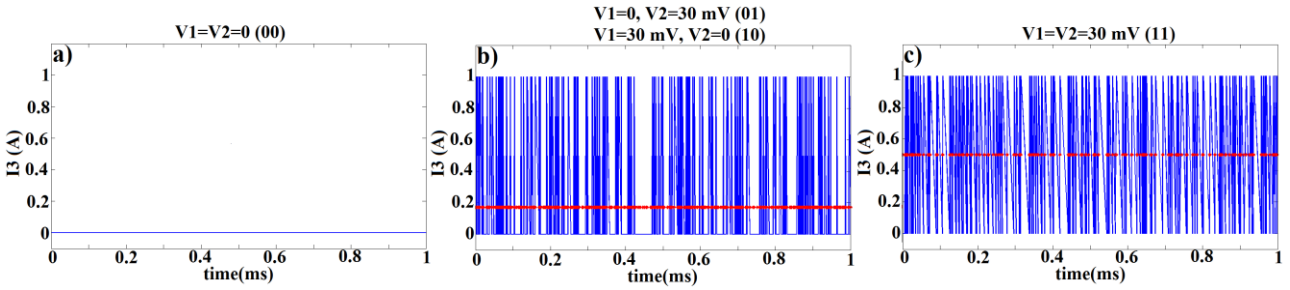

Fig. 7. Simulation results of output (current of contact 3: I3), where blue is instantaneous and red is the average current during 1 ms of time for input states of: a) 00, b) 01/10, and c) 11.

A very important point is the perspective that the bi-potential diagram method provides about the behavior of single electrons. This technique offers a simple way for the designers to introduce and to optimize complex SEDs. Moreover, it delivers the physical origins of electron transfer in SEDs, and is able to describe time analysis. The output current of the designed SEA gate is equal to:

$$I_3 = \frac{V_{eff}}{R} \tag{8}$$

where V_{eff} is the voltage difference that the electron feels in the direction of its movement and R is the resistance of the tunnel junction in the output path. So, the tunneling time of a single electron can be calculated as follow:

$$t = \frac{e}{I_3} = \frac{eR}{V_{eff}} \tag{9}$$

In state 11, for an electron, transferring from contact 3 to the island and from the island to one of the contacts of 2 or 1, the transient analysis can be calculated as:

$$t = \frac{200k\Omega \times 1.6\times10^{-19}}{1.25mV} + \frac{200k\Omega \times 1.6\times10^{-19}}{18.75mV} = 25.6ps + 1.708ps = 27.308ps \tag{10}$$

It means that 25.6 ps takes for electrons to jump from island to V1 or V2, and 1.708 ps is needed for an electron to tunnel from V3 to island. Therefore, 27.308 ps is the minimum time for the designed SEA gate to response to the inputs, and maximum available frequency of this gate is $F_{Max} = 1/(27.308 \times 10^{-12}) = 36.619\ GHz$.

Moreover, this analysis shows that this SED can be faster if the tunneling time of electron from island to V1/V2 gets lower (by reducing tunneling resistances of R_1 or R_2, or by increasing effective voltage of island-V1/V2). These points of views are neither available in conventional methods, nor with SIMON software

3. Simulation results

In this section, the output is simulated with SIMON software for the input states of the designed SEA gate. As expected, in the input state of 00, the output current is zero (output state is 0). In input states of 01 and 10, the average output current is small (output state is 0). In input state of 11, the tunneling rate is greatly increased (the average output current is about 2.5 times of the 01 or 10 states), and the output state is changed to 1.

These results approve the right operation of the designed SEA gate. Besides, by comparing the predictions of bi-potential method with simulations of SIMON, the bi-potential technique is confirmed, while provides the mentioned advantages.

4. Conclusion

In this article, first, a physical view of the structure and how to make single electron devices (SEDs) were explained. Then the equivalent circuit and structure of a single electron AND (SEA) gate was designed. Afterwards, the bases of bi-potential diagram method were provided, and it was employed to design the performance of introduced SEA. The coulomb blockade phenomenon was investigated via bi-potential diagram, and the time analyses were carried using it. It was shown that this method is based on the physics of the electrons, and is able to provide advantages for engineering SED applications. Moreover, the results of the designed SEA gate were confirmed with SIMON software.

5. References

[1] M. J. Sharifi and K. Jamshidnezhad, “A general SPICE compatible circuit model for single-electron devices and application to bit-error-rate calculations”, *Int. J. Circ. Theor. Appl.*, vol. 42, no.8, pp. 769-793, 2014.

[2] Y. S. Yu, S. W. Hwang, and D. Ahn, “Macromodeling of Single-Electron Transistors for Efficient Circuit Simulation”, *IEEE TRANSACTIONS ON ELECTRON DEVICES*, vol. 46, no. 8, pp. 1667-1671, 1999.

[3] M. J. Sharifi, “Transient Response of Single-electron Devices and Their Time Constants”, *Journal of the Korean Physical Society*, vol. 58, no. 1, pp. 138-149, 2011.

[4] Davoud Bahrepour and Mohammad Javad Sharifi, “A New Single Electron Tunneling Cell Based on Linear Threshold Gate”, *AIP Conference Proceedings*, vol. 1341, no. 1, pp. 148-152, 2011.

[5] F. Zhang, R. Tang, Y.-B. Kim, “SET Based Nano Circuit Simulation and Design Method Using HSPICE”, *Microelectronics Journal*, vol. 36, no. 8, pp. 741-748, 2005.

[6] Lageweg, S. Cotofana¸ and S.Vassiliadis,“Evaluation-methodology-for-single electron encoded Threshold logic gates”, *IFIP International Federation for Information Processing*, pp. 247-262 , 2006.

[7] Mohammad Javad Sharifi, “A Theorical Study of Performance of a Single-Electron Transistor Buffer”, vol. 94, no. 6, pp. 1105-1111, 2011.

[8] Takada, Shintaro, Hermann Edlbauer, Hugo V. Lepage, Junliang Wang, Pierre-André Mortemousque, Giorgos Georgiou, Crispin HW Barnes et al., “Sound-driven single-electron transfer in a circuit of coupled quantum rails”, *Nature communications*, vol. 10, no. 1, 2019.

[9] Gholinejad, Jalal, Kian Jafari, and Kambiz Abedi, "Optical XOR Interconnect Gate Based on Symmetric and Asymmetric Plasmonic Modes in IMI Structure Using Modified Kretschmann Configuration", 2019 2nd West Asian Colloquium on Optical Wireless Communications (WACOWC), IEEE, 2019.
[10] Maillet, Olivier, Paolo A. Erdman, Vasco Cavina, Bibek Bhandari, Elsa T. Mannila, Joonas T. Peltonen, Andrea Mari et al., "Optimal probabilistic work extraction beyond the free energy difference with a single-electron device", *Physical review letters*, vol. 122, no. 15, 2019.
[11] Pekola, Jukka P., and Ivan M. Khaymovich, "Thermodynamics in single-electron circuits and superconducting qubits", *Annual Review of Condensed Matter Physics*, vol. 10, pp. 193-212, 2019.
[12] Iwata, Yoshiaki, Tomoki Nishimura, Alka Singh, Hiroaki Satoh, and Hiroshi Inokawa, "High-frequency rectifying characteristics of metallic single-electron transistor with niobium nanodots", *Japanese Journal of Applied Physics*, vol. 61, no. SC, 2022.
[13] Darwin, S., E. Fantin Irudaya Raj, M. Appadurai, and M. Chithambara Thanu, "A Detailed Study on Single Electron Transistors in Nano Device Technologies", In Energy Systems Design for Low-Power Computing, IGI Global, pp. 67-99, 2023.