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A Low-Noise Low-Power Chopper Amplifier With 130dB CMRR and High SNR

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Abstract
This paper presents a low-power and low-noise chopper amplifier for biopotential signals. A two-stage structure is presented to achieve a high CMRR and SNR. These stages contain a folded cascode topology to obtain a low input noise and large input impedance; and a stage of two stacked cross-coupled folded cascode for CMRR and SNR intents. The structure consumes 1.27 µW from a 0.6 V power supply. The CMRR, SNR, Gain, and input-referred noise RMS respectively are 133 dB, 121.4 dB, 38 dB and 930nV/Hz in the Bandwidth of 0.01 kHz to 1 kHz. The NEF and PEF are 1.8 and 1.9 and input impedance is 2.5 GΩ with chopping frequency of 2kHz.

Keywords
Chopper amplifier, low noise, low power.

1. Introduction

Wearable and implantable devices have grown much attention due to their ability to track and monitor body conditions without being sensed. This ability, however, requires low power consumption, low self-created noise, and a tiny chip area usage [1]. Due to the need for input impedance matching to decrease return losses [2], achieving an input impedance of over 100MΩ has been a challenging issue [3]. In order to decrease the power consumption, reducing the power supply can be done, however, the circuit complexity will increase. Nowadays subthreshold designs, due to their efficiency in decreasing current usage, received growing demands to solve the power consumption issue with the cost of low transistor speed [4]. In the subthreshold region, although the bandwidth is very low, limiting the operation of the amplifier, the bio signal inputs of these amplifiers also have a low frequency. Therefore, this region is valuable for biomedical uses [5]. The bio signals also have a low amplitude. Normal amplifiers, cannot be beneficial in this issue; because of their large internal and self-created noises. Thus, in this matter, the chopping technique is suggested. This method contains two phases of frequency transfer that remove the noise and offset created along the operation. By filtering this noise, there will be a clear amplified signal in the output [6]. The block diagram of a basic chopper amplifier is displayed in Fig. 1.

Owing to the significance of noise and its incidence in biomedical applications, to have an obvious vision, a specific parameter has been introduced in [7], Noise Efficiency Factor. Noise Efficiency Factor (NEF) turns large numbers into visible and comparable cases.

$$NEF = V_{n,rms}\sqrt{\frac{2I_{tot}}{\pi V_T 4kT.BW}} \quad (1)$$

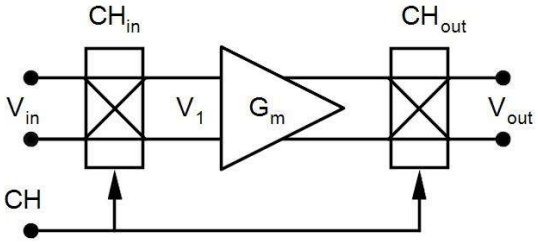

Fig. 1. Simple Chopper Amplifier Schematic

that $V_{n,rms}$ is total rms input-referred noise, I_{tot} is the current drawn by the entire system, k is Boltzmann constant that is $\sim 1.38 \times 10^{-23}$ and BW is the Band Width of the system in Hertz.

If two amplifiers had the same current and noise, they would have the same NEF, even if they have different Vdd. Therefore, another factor, PEF, has been presented in [8], that is described in (2):

$$PEF = NEF^2.Vdd \quad (2)$$

To decrease the NEF and area of the chip, a structure of stacked transistors has been proposed for neural recordings [9]. In [1], the stacking has been done with blocks of inverters. These methods are for the current mode structures. For voltage mode on the other hand, [10] and [11] have introduced a dual chopper and dual-path structure. Having two or more paths for a signal causes more SNR, CMRR, and PSRR. However, these structures have more complexity because of multiple chopping frequencies without overlapping. In this case, if frequencies overlap, the main signal, thereby the important information, will be changed or even disappeared.

This paper presents a Capacitively Coupled Chopper Instrumental Amplifier (CCIA) with optimization in power consumption. Also, a dual path in base frequency has been added to achieve a high CMRR and SNR.
The amplifier blocks are fully differential, which enhances their low-noise performance According to reference [12].
This paper is organized as follows. In section 2, the block diagram of the architecture has been discussed, the 3'd section represents each block's designs in detail. The measurement results are given in section 4 and finally, in section 5 there will be a conclusion around reached results.

2. Circuit architecture

The block diagram of the proposed structure is presented in figure 2. The circuit consists of a chopped pre-amplifier, Gm1, followed by a two-path parallel structure. The signal passes through both paths and gets amplified and then added together.

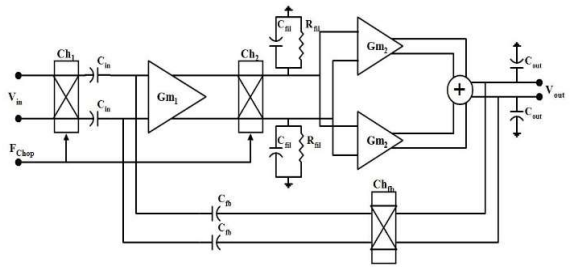

Fig. 2. Block Diagram of Proposed Chopper Amplifier

In order to decrease input offset, after the first chopping stage, input capacitors have been placed. The first phase of amplifying is done in chopping frequency. Therefore, the input offset and noise have been transferred to upper frequencies. This operation is the traditional part of the circuit. The amplifier is offered in [13]. After demodulating to the baseband and the first filtering, two paths of folded cascode amplifiers take the role of post-amplifying and increasing CMRR and SNR. The second amplifier is introduced in [11]. Furthermore, for using the two signals amplified by each path in the main path, an adder has been used. Afterward the output is filtered by capacitors again.
If A_1 and A_2 can be considered for Gm_1 and Gm_2 open-loop gain, there will be $A_{v,\,total}=2A_1A_2$, so the open-loop gain is high enough to have an excellent closed-loop gain accuracy.
For closed-loop gain, the input and feedback capacitor amounts are required. In this work, the capacitors are C_{in}=20p and C_{fb}= 250fF, so for the gain: $A_v = 20\log(C_{in}/C_{fb}) = 38dB$.

3. Circuit's block design

In this section, design of circuits and some of their characteristics will be presented.

3.1. First Stage Amplifier

The first stage amplifier is a recycling folded cascode (RFC) shown in Figure 3. As mentioned in [13] and [14], all transistors are biased in the subthreshold region for having a better power characteristic.

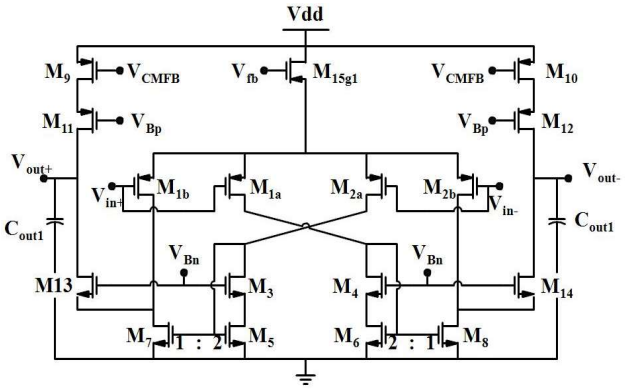

Fig. 3. First stage Amplifier (Gm1)

Differential Gain

In order to calculate the open-loop gain of the amplifier, we have

$$A_v = G_m . R_{out} \tag{3}$$

as mentioned in [13], the transconductance of RFC is:

$$G_m = (1 + \mathrm{k})g_{m,1a} \tag{4}$$

that $g_{m,1a}$ is g_m of M_{1a} here, and k is the ratio of M_7 and M_5 transistors sizes. so, there will be:

$$G_m = 3g_{m,1a} \tag{5}$$

And output impedance can be calculated as (6). Also, the amplifier's differential gain can be expressed by (7).

$$R_{out,diff} = r_{o,13}.g_{m,13}(r_{o,7} \| r_{o,1b}) \| (r_{o,11}.r_{o,9}.g_{m,11}) \tag{6}$$

$$A_{V,diff} = 3g_{m,1a}.(r_{o,13}.g_{m,13}(r_{o,7} \| r_{o,1b}) \| (r_{o,11}.r_{o,9}.g_{m,11})) \tag{7}$$

Common-mode Gain

For Common-mode gain same roles are true. G_m is equal to $3g_{m,1a}$ and A_v is equal to G_mR_{out}.
As for R_{out}:

$$R_{o,CM} = \frac{1}{4} r_{o,13}.g_{m,13}(r_{o,7} \| r_{o,1b}) \| \frac{1}{2}(r_{o,11}.r_{o,9}.g_{m,11}) \tag{8}$$

And the Common mode gain is:

$$A_{V,CM} = 3g_{m,1a}.(\frac{1}{4} r_{o,13}.g_{m,13}.(r_{o,7} \| r_{o,1b}) \| \frac{1}{2}(r_{o,11}.r_{o,9}.g_{m,11})) \tag{9}$$

A. CMRR

Common Mode Rejection Ratio (CMRR) of an amplifier is:

$$CMRR = \frac{A_{v,Diff}}{A_{v,CM}} \tag{10}$$

For the first amplifier block:

$$CMRR_{G_{m1}} = 2\frac{r_{o,13}.g_{m,13}(r_{o,7} \| r_{o,1b}) + 2(r_{o,11}.r_{o,9}.g_{m,11})}{r_{o,13}.g_{m,13}(r_{o,7} \| r_{o,1b}) + (r_{o,11}.r_{o,9}.g_{m,11})} \tag{11}$$

3.2. Common mode Feedback

For setting common mode voltage in output on a proper amount, a common mode feedback (CMFB) is used (figure 4).

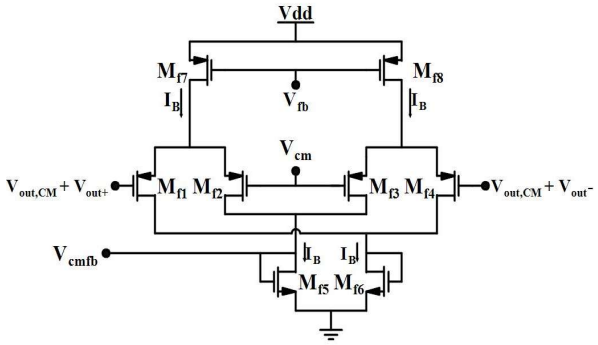

Fig. 4. The CMFB Circuit

In this circuit, the ideal form is the output common-mode in Gm1 equal to V_{fb}. Under some conditions, if one of the outputs, V_{out+} or V_{out-}, have an extra DC voltage on it, the CMFB circuit will operate.

(12) and (13) equations can be written for the currents.

$$I_{Mf2} = \frac{I_B}{2} + \Delta I \quad (12)$$

$$I_{Mf3} = \frac{I_B}{2} - \Delta I \quad (13)$$

Where, ΔI is the large signal changes on $M_{f2,3}$. For M_{f5} current (14) can be written.

$$I_{Mf5} = I_{Mf2} + I_{Mf3} = \left(\frac{I_B}{2} + \Delta I\right) + \left(\frac{I_B}{2} - \Delta I\right) = I_B \quad (14)$$

Thus, if the outputs are equal, no changes will happen in I_B, so the output current will be the same, whether differential signals are negative or positive.

If the CM voltage on one of the outputs becomes larger than V_{fb}, the current on $M_{f3,4}$ will increase. Thereby I_{M5} will grow larger and sets the bias voltage of V_{cmfb} that is connected to $M_{9,10}$ in figure 3. This reduces their currents. So, the output CM voltage will be back to V_{cm} [15].

3.3. Second stage Amplifier

The second stage amplifier (Gm2), with a cross-coupled folded cascode topology, is presented in Figure 5.

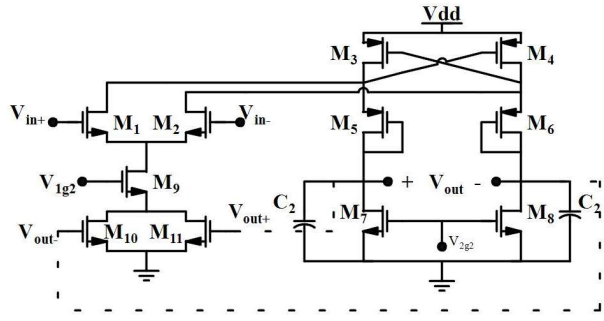

Fig. 5. Second stage amplifier

In order to have larger transconductance, low noise, and less power consumption, all the transistors are biased in the subthreshold region. The input transistors are kept big enough to obtain the low power goal. Transistors M10 and M11 are operating as CMFB of this amplifier. Their two gates are connected to outputs and they control the current flowing in the circuit and set the output common-mode [10]. As reported in [16], to boost bandwidth, M3 and M4 have become cross-coupled and M5,6 diode connected.

Differential Gain

For the first half of amplifier, the gain calculates

$$A_{v,diff1} = G_{m1} \cdot R_{out1} \quad (15)$$

$$R_{out1} = \frac{-1}{g_{m3}} \parallel \frac{1}{g_{m5}} = \frac{-1}{g_{m3} - g_{m5}} \quad (16)$$

$$A_{v,diff1} = \frac{-g_{m1}}{g_{m3} - g_{m5}} \quad (17)$$

Whereas, g_{m1} is high enough to provide a good differential gain.

And for the second half, the gain is (18).

$$A_{V,diff2} = \frac{r_{o,9}}{r_{o,9} + \frac{1}{g_{m,5}} + \left(\frac{1}{g_{m,3}} \parallel r_{o1}\right)} \square \frac{r_{o,9} \cdot g_{m3} \cdot g_{m,5}}{r_{o,9} \cdot g_{m3} \cdot g_{m5} - g_{m,5} + g_{m,3}} \quad (18)$$

Therefore, the main differential gain is as (19) and (20):

$$A_{V,diff\ (G_{m2})} = A_{V,diff_1} \times A_{V,diff_2} \quad (19)$$

$$A_{V,diff\ (G_{m2})} = -\frac{r_{o,9} \cdot g_{m,3} \cdot g_{m,5}}{(g_{m,3} - g_{m,5}) \cdot (r_{o,9} \cdot g_{m,3} \cdot g_{m,5} - g_{m,5} + g_{m3})} \quad (20)$$

if $r_{o9} \cdot g_{m3} \cdot g_{m5}$ be high enough, the gain can be expressed as:

$$A_{v,diff} \simeq A_{v,diff1} \quad (21)$$

Common-mode Gain

The way of calculating is the same as differential gain:

$$A_{v,CM1} = \frac{R_{d1}}{\frac{1}{g_{m1}} + R_{S1}} \quad (22)$$

Where, R_{d1} is the impedance on Drain and R_{s1} is on the Source of M1,

$$A_{v,CM1} = \frac{-1}{(1 + r_{o9} g_{m1}(1 + g_{m10} r_{o10}))(g_{m3} - g_{m5})} \quad (23)$$

$A_{v,\,CM2}$ is the same as $A_{v,\,diff2}$, so the circuit common mode gain can be described as (24):

$$A_{V,CM(Gm2)} = \frac{-r_{o,9} \cdot g_{m,3} \cdot g_{m,5}}{(r_{o,9} \cdot g_{m,3} \cdot g_{m,5} - g_{m,5} + g_{m,3})(1 + r_{o,9} \cdot g_{m,1} \cdot (1 + g_{m,10} r_{o,10}))(g_{m,3} - g_{m,5})} \quad (24)$$

Due to the large denominator of this equation, it is clear how this structure lowers the common-mode gain and causes large CMRR.

3.4. Adder Block

The adder schematic is presented in Fig. 6.

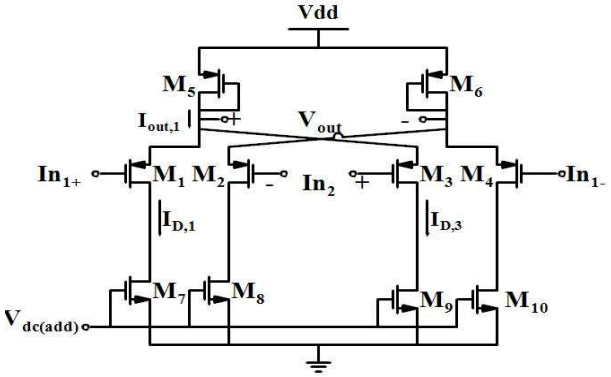

Fig. 6. Adder schematic

For this circuit (25) and (26) are true:

$$I_{out1} = I_{D,1} + I_{D,3} \quad (25)$$

$$V_{out,1} = I_{out,1} \times \frac{1}{g_{m,5}} \quad (26)$$

Since the transistors are in saturation mode, the currents are:

$$I_{D,sat} = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}(V_{gs} - V_{th})^2 \quad (27)$$

Indeed, $V_{gs} \propto V_{in}$, so for the output $V_{out} \propto V_{in1} + V_{in}$.

3.5. Voltage Reference

The Voltage Reference presented in this paper is shown in figure7 [17]:

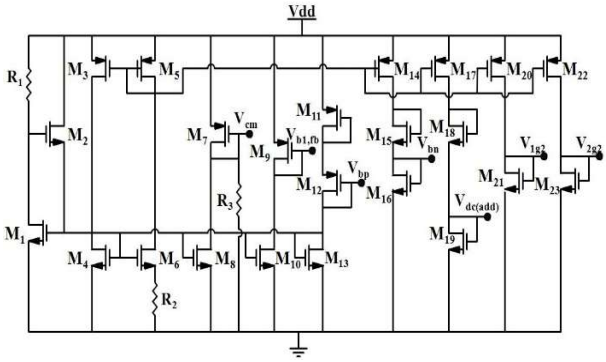

Fig. 7. Voltage Reference

In this circuit, the voltage needed in the whole circuit, containing two amplifiers, one adder, and common-mode feedback has been produced in order to lower the power consumption. All transistors are biased in the subthreshold region. Transistor and resistor sizes are offered in table I:

Table I Sizes of Voltage Reference Circuit

Component	Size(μm/μm)	Component	Size(μm/μm_kΩ)
$M_{1\text{-}7}$	2/0.18	M_{20}	0.45/0.18
M_8	2/0.3	M_{21}	0.43/0.2
M_9	12/0.54	M_{22}	0.22/0.18
M_{10}	1.6/0.18	M_{23}	45/0.18
$M_{11,12}$	1/0.18	R1	1
M_{15}	2.6/0.2	R2	1
M_{16}	0.25/0.18	R3	100
M17	0.25/0.18		
M_{18}	1.4/0.18		
M_{19}	0.22/0.18		

As for same size of M_3-M_6, current flowing in each branch is the same. To have different voltages, the additional transistors must take part. The circuit generates seven voltages, V_{cm} for CMFB, $V_{b1,\,fb}$ for Gm_1 and CMFB at the same time, V_{bp} and V_{bn} for Gm_1, $V_{dc(ad)}$ for adder and V_{1g2} and V_{2g2} for Gm_2. Each voltage is independent from others. Obviously, changes in one don't cause a change in others.

3.6. Pulse Generator

A standard non-Overlapping clock generator is shown if Fig. 8 below [18]:

If the first moment is assumed, both outputs are logically zero, for the input equal to one, the output of $NAND_1$ gate will be high according to its logic described in Table II.

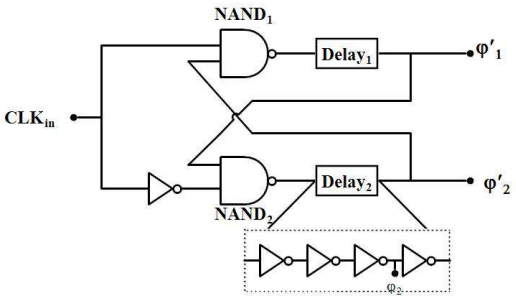

Fig. 8. Clock Generator Block

Table II NAND Logic

A	B	Out
0	0	1
1	0	1
0	1	1
1	1	0

Where A and B are NAND inputs.

In order to have non-overlapping clock waves, delay blocks including NOT gates are being used. After facing the delay block, the first output, φ_1, followed by φ'_1, will be acquired. also, the same analyses are valid for the second pat. So, φ'_1 and φ'_2 have inverted forms of each other.

φ_1, φ_2, φ'_1 and φ'_2 will be the clock inputs of Chopper Blocks.

3.7. Chopper Blocks

The chopper modulator used in the suggested design is shown in Fig. 8 [19].

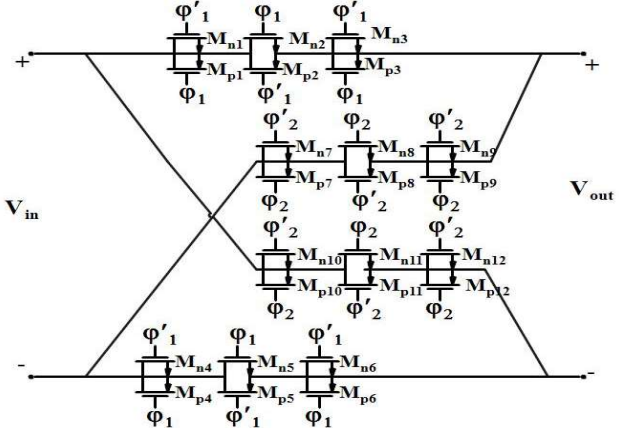

Fig. 9. Chopper Modulator block

In order to reduce the effect of charge injection observed in usual choppers, the chopper used in this structure contains transistors differentially connecting, to reject the injected charge as common-mode voltage, as a result of matching transistors. Furthermore, in each row, there is two half-sized dummy switches to force the channel charge to divide by the same amount between source and drain and compensate for the injected charge [20].

4. Simulation results

The proposed circuit is designed in 0.18um TSMC CMOS

technology in Spectre simulator. As a result of applied changes on the base circuit, as mentioned previously, the

AC gain and the bandwidth have been increased to 37dB in 1kH (from 0.01Hz to 1khz), additionally, the unity-gain bandwidth is 9kHz with a phase margin of 80 degrees. The AC of this circuit with an input of a 50 Hz (For EEG and ECG applications) sinusoid is shown in figure 10.

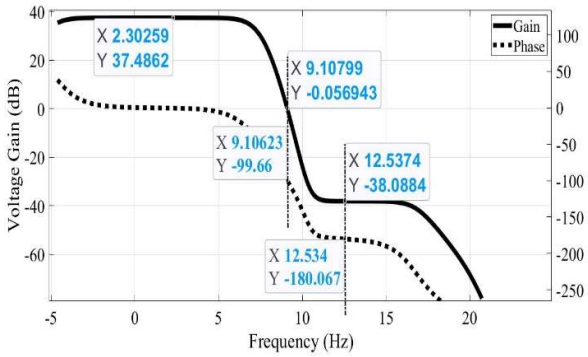

Fig. 10. AC response of closed loop Circuit

The transient response of this circuit is presented in Fig. 11. In order to have a better view of waves created during the loop, the output of the first amplifier before demodulation (Gm_1 mod and dem), the input wave, and the final output are given in this figure 11-a. Furthermore, to have a better look at output ripple, a magnified part is added to the figure (11-b).

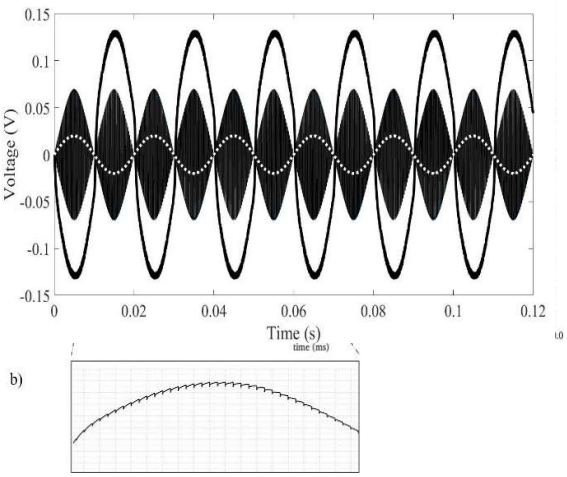

Fig. 11. Transient Results. (a) The main results, (b) Zoomed image of output

The CMRR and PSRR of this circuit are shown in Fig. 12. Both of them have flat curves in a part of the bandwidth. PSRR is 33dB at full bandwidth and CMRR, in this frequency band, is more than 90 dB with a maximum of 133dB. These two shows that this circuit rejects the input and the power supply interference signals nicely.
In chopping frequency, the noise floor is 250nV/√Hz, and RMS of the curve in bandwidth (0.01-1kHz) is 930nV. For better realization of noise performance, NEF, will be calculated [7]. The current consumption of whole circuit is 2.8μA, so the NEF will be 1.8. In addition to this, PEF can be calculated with this amount which is 1.9.

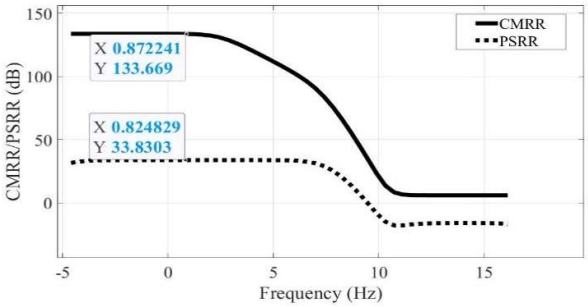

Fig. 12. CMRR and PSRR

Figure 13 presents the noise performance of this circuit.

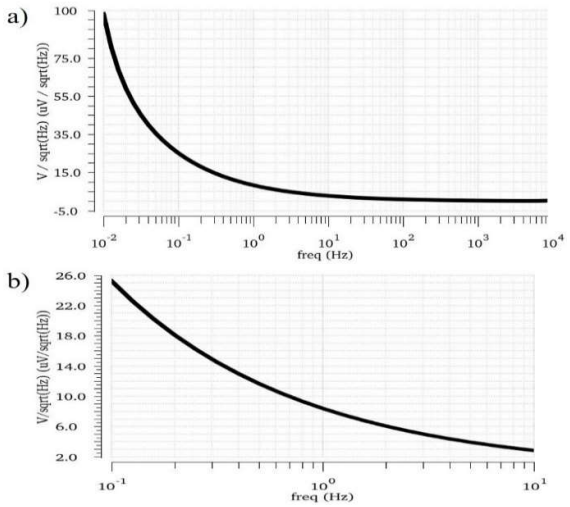

Fig. 13.a) Input-Referred Noise; b) Input-Referred Noise in 0.1-10 Hz Range

Power and SNR Monte-Carlo simulation results are shown in Fig. 14.

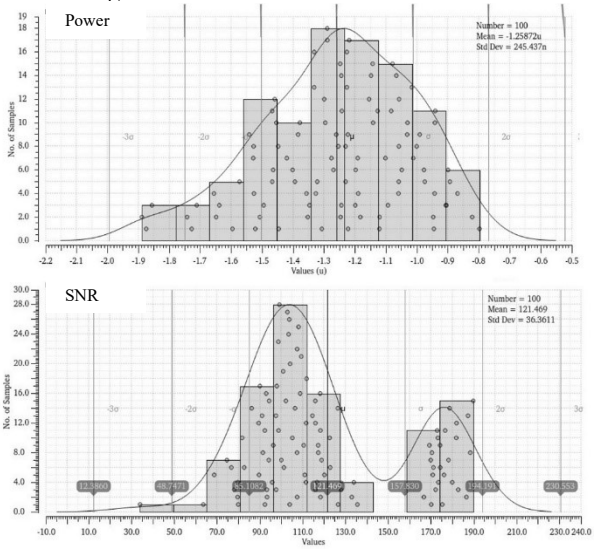

Fig. 14. Monte-Carlo Simulation

It can be seen from histograms that for 100 samples, power consumption mean amount is 1.27μW and its standard deviation (std dev) is 245.4 nW. As for SNR, mean amount is 121.4dB and Standard Davison is 36.3dB. It should be noted that in these histograms, the mean is the

most possible amount between 100 samples and std dev is variation of the samples around the mean value. So, in this case, the most expected value for power consumption and SNR are 1.27μW and 121.4dB.
As for the power, this range of amount was expected with regards to $I_{dc} \times Vdd$ which is 1.6μW with simple calculations. The corners simulation results in room temperature are presented in table III:

Table III Corner Analyses

Corners Output	Fast-Fast (FF)	Slow-Slow (SS)	Fast-Slow (FS)	Slow-Fast (SF)
AC Gain (dB)	31.7	34	37	32
Phase Margin (degree)	77	67	61	63
RMS noise (μV/√Hz)	1.1	6.2	1.1	5.5
Power (μW)	3.02	0.61	1.08	1.4
SNR (dB)	114	97	91	108
Max-CMRR (dB)	70	75	140	80
Max-PSRR (dB)	29.25	31.15	35.89	29.39

In these corners, all the numbers are in acceptable range and close to each other.
Finally in Table IV there will be a comparing between this work and other papers.
There is a trade-off between power, Bandwidth, and noise. The less power consumption, the more input-referred noise. Although the bandwidth has a reverse ratio to the noise efficiency factor and more bandwidth causes less NEF, the noise RMS and the Current flown in the circuit are also related to it directly. So, the trade- off between these three should be considered for a better NEF.

5. Conclusion

In this paper, A Low power and low-noise chopper amplifier for ECG and EEG applications has been recommended. The proposed structure has two stages. the first stage uses a folded cascode and the second stage is two current re-use folded cascode. it can be concluded that the structure has better noise and power performance while having a similar performance for CMRR and gain.

Table IV proposed Chopper Amplifier Performance Comparison with Previous Work

Title	This Work	[11]	[13]	[21]	[22]	[23]	[24]	[25]
Technology (nm)	180	130	180	65	180	180	180	65
Supply(V)	0.6	0.7,1.2	0.6	1.8	3.3	5	1.21	1.2
Power(μW)	1.27	2.66(0.7v)3.26(1.2 v)	0.68	1.8m	481.8	5.03m	1.21	2
Gain(dB)	38	34 - 38	40.55	40	40.09	20	40	33.6-53.4
B.W. (Hz)	1k	4k – 3k	~330	~100k	39.2k	850k	800	~250
Noise RMS (nV_{rms})	930	3.16μ(min)to 6.83μ(max)	-	2.8	5.53	39	1800	-
NEF	1.8	-	-	3.38	2.9-3.22	-	5.4	7.8
CMRR (dB)	133	-	-	129	109	129	>108	-
SNR (dB)	121.4	89.06-92.85	-	-	-	-	-	-
Year	2023	2019	2019	2021	2021	2022	2022	2023

6. References

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