Tabriz Journal of Electrical Engineering (TJEE), vol. 54, no. 3, Autumn 2024 Serial no. 109
DOI: 10.22034/tjee.2023.58147.4705

A 147dBΩ, High Dynamic Range Analog Front End for PPG Signal Acquisition with Fine and Coarse Steps Automatic Gain Control

F. Shoeibi, E. Najafiaghdam*, A. Ebrahimi
Department of Electrical Engineering, Sahand University of Technology, Tabriz, Iran
E-mail addresses: f_shoeibi@sut.ac.ir, najafiaghdam@sut.ac.ir, aebrahimi@sut.ac.ir
*Corresponding author

Received: 26/08/2023, Revised: 14/11/2023, Accepted: 30/12/2023.

Abstract

This paper deals with the design of a low power, high-gain, low noise and high-dynamic range receiver dedicated for photoplethysmography (PPG) signal sensing. A current measurement system utilizing a large DC cancelation block, implemented in 180nm CMOS technology. The shunt feedback trans-impedance amplifier (TIA) is designed to detect and sense low currents, producing a voltage output. It exhibits a noise floor of 39.7 pArms within the frequency range of 0.5-10Hz. The receiver gain is 147.6dBΩ. The receiver incorporates a fine and coarse steps gain control block (FaCGC) and a DC cancelation block capable of handling up to 100μA, thereby enabling a wide dynamic range. The proposed system exhibits characteristics such as low noise and wide dynamic range, rendering it well-suited for the precise measurement of ultra-low current. Consequently, this system holds significant potential for application in biosensor technology. The chip has a footprint of 0.121mm2 area and operates with a power consumption of 40.14 micro-watts, drawing power from supply voltages of $\pm$0.9 volts. The post-layout simulation reveals a lower frequency limit below 1mHz, while the upper limits of its application band can be extended up to 100 Hz.

Keywords

Photoplethysmography, PPG signal receiver, Current to voltage convertor, Transimpedance, Automatic gain control, Background light rejection loop.

1. Introduction

2.

The recent increase in demand for wearable health monitoring systems has led to a rise in the application of photoplethysmography (PPG) sensors in portable and compact biomedical systems. The utilization of PPG sensors enables the acquisition of Photoplethysmography signals with the objective of monitoring heart rate, measuring blood pressure [1], recognizing emotions, and assessing cardiovascular disease. The PPG sensors utilize a light emitting diode (LED) to emit light onto the body, while a photodiode is used to receive the reflected light from the subject's body. As depicted in Fig. 1, it is necessary to employ a high-gain amplifier to amplify the weak current signal and subsequently convert it into voltage using a low-noise trans-impedance. This voltage conversion is performed to facilitate the filtering and transmission of the signal to the signal processing units.

The alternating current (AC) component of the PPG signal exhibits a significantly lower magnitude compared to the direct current (DC) component. The light in measurement environment can result in a DC component of photocurrent reaching levels as high as 100μA. Consequently, it is imperative for the Analog Front End (AFE) to possess the capability to effectively eliminate or mitigate this substantial DC component.

With this motivation, recently, the issue of design a low power and portable analog- front- end (AFE) for PPG sensors has attracted a great attention among researchers[2]–[6]. The quality of the sensed signal is influenced by the specifications of the designed AFE for the PPG sensor, including parameters such as gain, signal-to-noise ratio (SNR), and dynamic range.

Designing a PPG AFE presents several challenging issues. Primarily, the weak nature of the captured signal necessitates the design of a low noise circuit for the AFE. In order to ensure optimal performance, it is imperative that the noise floor of the receiver for the photoplethysmography signal remains below the threshold of 100pA/sqrt (Hz). The second significant concern pertains to power consumption, which assumes even greater significance when considering wearable devices. The third issue arises from the presence of background light (BGL), which introduces a significant DC component to the desired AC signal. Consequently, it is advantageous to employ a high-gain amplifier with a high signal-to-noise ratio. The presence of significant DC components in the input signal leads to rapid saturation of the current-to-voltage amplifier.

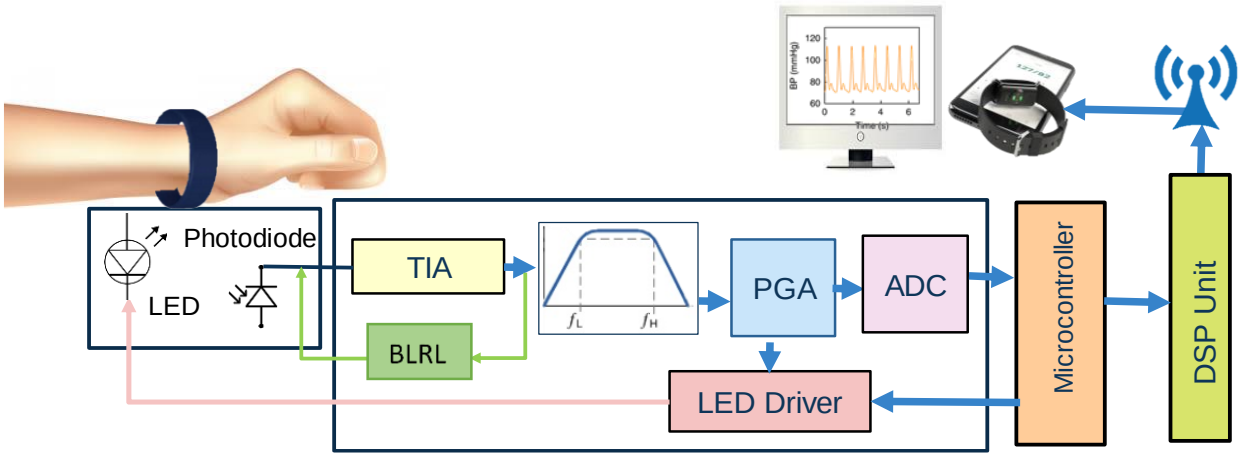


Fig. 1. The block diagram of a PPG Signal monitoring system.

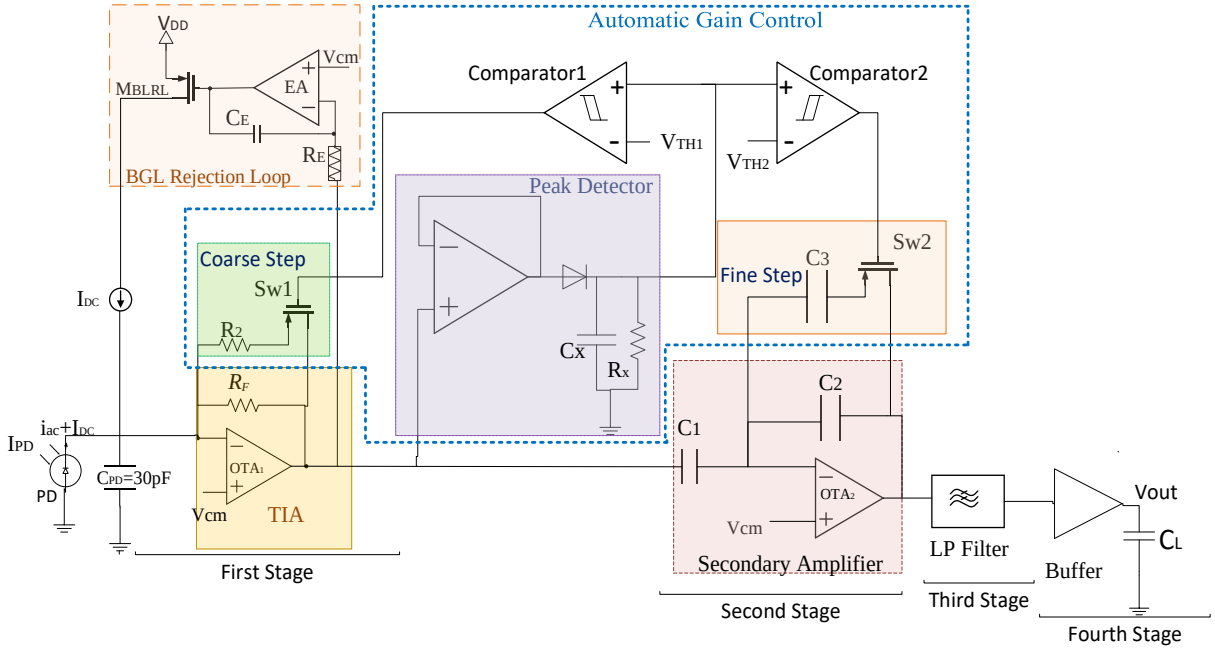


Fig. 2. The block diagram of proposed system.

In order to alleviate the disruptive impact of BL, several studies have employed a background light cancellation loop [7]–[9]. In another effort, a digitally controlled digital to analog converter (DAC) was employed to overcome this problem [10][11].Given that PPG signals typically fall within the frequency range of 0.5 to 10 Hz, it is important to consider the impact of flicker noise on these signals, as they possess extremely low amplitudes. Moreover, the subsequent task entails the design of a band-pass filter featuring a low cut-off frequency. The low cut-off frequency necessitates the utilization of high resistance and capacitance values, resulting in an augmented area cost. The low cut-off frequency requires large resistance and capacitance, which increase area cost. Several techniques were utilized to address this issue, including the implementation of α-block[5], Gm-C filters [12], off-chip elements. Based on the aforementioned notes, it is imperative to take into account all constraints during the design procedure of AFE for PPG sensor.

In this paper, we focused on designing the PPG receiver blocks before analog to digital converter (ADC). The design consists of TIA block, secondary amplifier and filter. The paper also addresses potential issues such as saturation due to DC photocurrent and distortion of the PPG signal, and implements solutions such as a background light rejection loop (BLRL) and an automatic gain control (AGC) scheme to enhance the dynamic range of the AFE.

3. PPG Front-End Architecture

This paper is an expanded presentation of the circuit initially introduced in [13]and[14]. The expanded system design takes into account an increased range for dc removal. Additionally, the circuit incorporates a two-level gain control block to prevent saturation of the transimpedance amplifier (TIA) and the second stage, thereby enhancing the dynamic range. The proposed AFE in this study has five blocks, each with a specific function.

As illustrated in Fig. 2, The first stage, TIA, has a high transimpedance gain of 122.8 dBΩ and converts the weak photocurrent from PD into voltage This stage also includes a background light rejection loop (BLRL) to suppress the input DC photocurrent, which can cause the high gain TIA to be saturated. The dc cancelation loop in our design can cancel the dc currents up to 100µA. The second stage employs capacitive feedback and has a closed-loop gain of C1/C2. This stage provides the gain of 25dB. In the third stage, a low-pass filter is implemented to reject noise at high frequencies. A unity-gain buffer is used in the fourth stage to test the off-chip load.

The AFE must be high-gain and low-noise in order to detect weak photocurrents, However, if the DC photocurrent due to BGL is not addressed, the large transimpedance gain of TIA can easily lead to saturation. As a result, a BGL rejection loop is designed to reject the DC photocurrent. Additionally, an AGC scheme with fine and coarse steps is implemented to control the gain of receiver in two levels when the photocurrent is very large, preventing distortion of the PPG signal. This enhances the AFE's dynamic range.

To achieve an extremely large time constant for a filter with a low-frequency corner, the resistance of RE must be very large. The pseudo-resistor is used in the (BLRL) block to maintain a low cut-off frequency less than mHz. The proposed circuit is designed and simulated in 0.18µm CMOS technology.

3.1. Trans-Impedance Design

Many different trans-impedance amplifier (TIA) topologies have been reported in literatures for biosensors and biomedical applications [15]–[17]. A valuable effort has been made to conduct a comparative study on several TIA topologies in order to provide a suitable choice for biomedical application. All TIA topologies were designed and simulated based on two scenarios; one for minimum power consumption and the other for minimum input noise. The evaluation is carried out in accordance with the TIA gain, input noise, power, and dynamic range merit indices [18]. The proposed system in this paper used a resistive shunt feedback trans-impedance.

The reflected photocurrent from the finger, arm, or wrist is received by the photodiode, and the weak photocurrent is converted to voltage by the TIA. The AC component of this photocurrent ranges from 0.1nA to 500nA and is proportional with blood volume changes [10]. Furthermore, the photocurrent has a DC component ranging from 100nA to 10µA. This DC current combined with ambient light, can cause the TIA to become saturated. Therefore, the TIA should be a low noise, high gain amplifier in order to improve the resolution of the acquired signal.

2.1.1. The TIA Core Amplifier Design

The core amplifier for shunt feedback TIA depicted in Fig. 3, which uses two complementary input pair to offer rail-to-rail input common mode range (ICMR). As a result, this topology improves the input ICMR by extending the NMOS input pair extends ICMR up to VDD and the PMOS input pair's ICMR down to VSS. The negative ICMR is limited to ICMR(-) $=VSS+VGS_{1,2(n)}+VDS_{tail(n)}$, whereas the positive ICMR is limited to ICMR(+) $=VDD-VSG_{1,2(p)}+VSD_{tail(p)}$; where the $VGS_{1,2(n)}$ is voltage gate to source of NMOS input pair and $VSG_{1,2(p)}$ is voltage source to gate of PMOS input pair. The $VDS_{tail\ (n)}$ and $VSD_{tail\ (p)}$ refer to the voltage that the NMOS and PMOS tail MOSFETS need to operate in saturation region. The DC sweep analysis in unity gain configuration for two-complementary input pairs is performed to evaluate the linearity region of OTA by varying the input voltage in the range of (-1V to 1V). In Fig. 4, the DC sweep result for both the PMOS and NMOS pair shows that the input and output voltage closely follow each other from -790mV to 790mV. The OTA1 has an open loop gain of 91.14 dB and a unity gain bandwidth of 3.64 MHz, which is sufficient for low frequency receivers. Post-layout noise simulation shows that the input referred noise is 19.16µVrms. The bias current of OTA1 is 1.2µA and it consumes 6.46µW power. The value of feedback resistor (R_f) is selected to be 1.43MΩ; Therefore, the TIA provides the gain of about 123dBΩ.

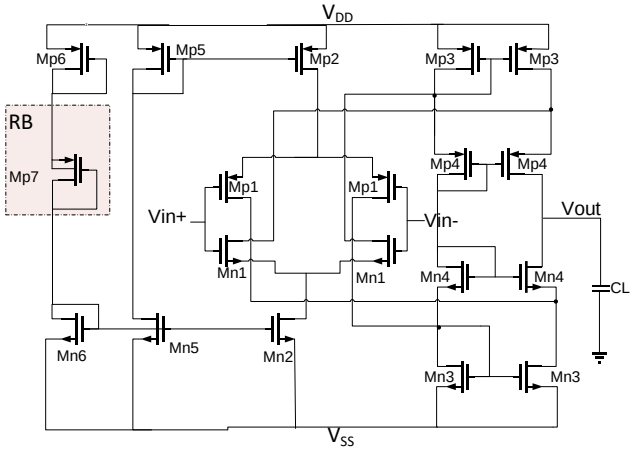


Fig. 3. High swing operational amplifier with bias circuit is used as core amplifier for TIA.

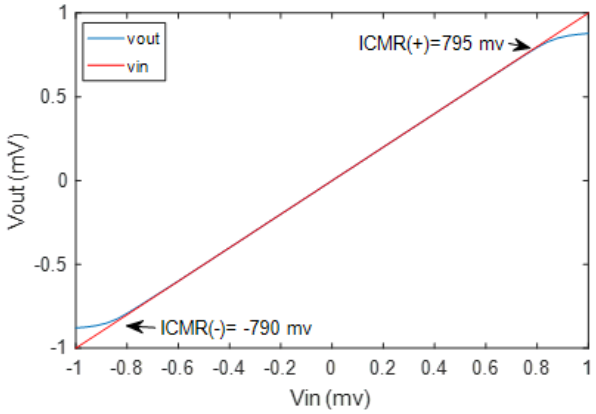


Fig. 4. DC sweep of V_{in} and V_{Out} for input MOS pair.

The design parameters for OTA1 and performance summery have summarized in Tabel1 and Tabel2, respectively.

Table I. W/L ratio of the MOS transistors of OTA.

Transistor	W/L(μm)
MN1	5.5/3
MN2, MP6	2.5/3
MN3	30/1
MN4	10/1
MN5, MN6	1.25/3
MP1	10/3
MP2, MP5	11/3
MP3	60/3
MP4	30/1.5
MP7	0.3/0.18

Table II. Summary performance of the core amplifier.

Parameter	Value
VDD (V)	± 0.9
I_B (μA)	1.2
Gain (dB)	91.14
Input referred noise(rms)(μV) @0.5-10Hz	19.16
P.M [Deg]	70
B.W (Hz)	116.7
Unity Gain Frequency (MHz)	3.64
Power(μW)	6.46
C_L	1pF

2.1.2. Background Light Rejection Loop (BLRL)

Background light rejection loop consists of an integrator and a PMOS transistor that is used to remove large DC components caused by ambient light. The integrated TIA output DC voltage was compared to VCM. If the TIA becomes saturated, the output of the error amplifier rises to a high value, and the MBLRL transistor turns on and sinks the current, resulting in DC photocurrent rejection.

2.1.3. Performance Equations

Fig. 5 shows a block diagram of two first-stage receivers. Ignoring the AGC unit and the BLRL loop, the TIA block's transfer function can be derived from the small signal model as shown in (1):

$$I_{in} = -\frac{(A+1)}{AR_f} V_{OUT1} \quad (1)$$

Where, A is the open-loop gain of input opamp and R_f is the feedback resistance. From (1), if A is sufficiently large (A>>1), the TIA gain can be simplified as follows:

$$Z_{TIA} = \frac{V_{OUT1}}{I_{in}} = -R_f \quad (2)$$

Given (2), the value of the shunt feedback resistor (R_f) is chosen to be 1.43MΩ in order to meet the high gain requirement. Because a high-gain TIA with a large PPG DC component can easily become saturated, an error amplifier with capacitive feedback and a pseudo-resistor was used to reject the large DC photocurrent at the TIA's input. The transfer function of TIA can be extracted from (3) to (7) using the BLRL loop.

$$V_G = -A_2 V_x \quad (3)$$

$$\frac{V_x - V_{OUT1}}{R_E} + (V_x - V_G) C_E S = 0 \quad (4)$$

$$I_{in} - g_{m(BLRL)}(V_G) = I_x \quad (5)$$

$$I_x = \frac{-V_{OUT1}}{R_f} \quad (6)$$

By substitution of V_x from (3) in (4), and replacing V_G and I_x in (5), the final transfer function of TIA can be written as (7):

$$Z_{TIA}(S) = \frac{-R_f(1+C_E S R_E(1+A_2))}{1+C_E S R_E(1+A_2)+g_{m(BLRL)}A_2 R_f} \quad (7)$$

The high pass corner frequency is estimated based on dominant pole. The -3dB bandwidth of the system is determined as (8):

$$f_{-3dB} = \frac{1+g_{m(BLRL)}A_2 R_f}{2\pi C_E S R_E(1+A_2)} \quad (8)$$

Where, $g_{m\ (BLRL)}$ is the transconductance of the transistor M_{BLRL}, A_2 is the open-loop gain of error amplifier.

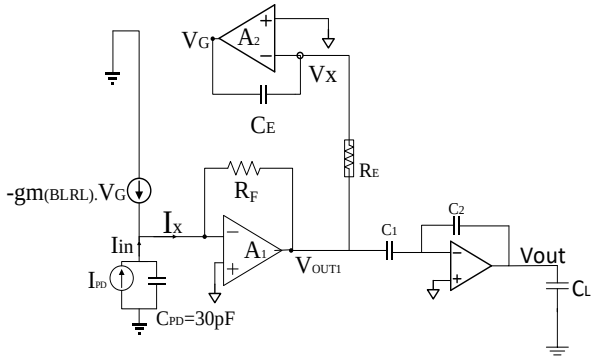


Fig. 5 Small signal model of two first stage.

The gain of the second stage, which is a capacitive feedback amplifier is determined by the ratio of C_1 and C_2 capacitors. By selecting the C_1 as 3.4pF and C_2 as 200fF, the second stage provides the gain of 24.6dB. For the capacitive feedback amplifier and others in the next stages we use the same OTA shown in Fig. 3.

Because of the small current of the photodiode and the low frequency bandwidth of the PPG receiver, the noise level must be very low in order to operate at high sensitivity. The main source of noise in TIA arises from the thermal noise of feedback resistor (R_f), the noise of MOS transistors in the first stage OTA, the noise of M_{BLRL} and the flicker noise of the input pair transistors which is the dominant noise in low frequency application. The low frequency input-referred noise current for shunt feedback TIA is given by [19]:

$$\overline{i_{n.in}^2} = \frac{\overline{V^2_{n.amp}}}{{R_f}^2} + \overline{i^2_{n.M(BLRL)}} + \overline{i^2_{n.R_f}} \quad (9)$$

$$\overline{V^2_{n.amp}} = \frac{4kT\gamma}{(gm_n+gm_p)} + 2\overline{V^2_{n.flicker}} \quad (10)$$

$$\overline{V^2_{n.flicker}} = \frac{K_f}{C_{ox}WL} \times \frac{1}{f} \quad (11)$$

Where, k is the Boltzmann's constant, T is the temperature, γ stands for the noise factor of the transistors, gm_n and gm_p are the transconductance of the input transistors in core voltage amplifier, K_f is process dependent constant, W and L are width and length of NMOS and PMOS input pair transistors, f is frequency and C_{ox} is gate oxide capacitance. Since the PPG bio-signals are low frequency signals; therefore, the dominant source of noise affecting the PPG signal quality is flicker noise. Eq. (11) explains the inverse relationship between the flicker noise and the dimensions of MOS transistor. Hence, selecting a large value for length and width of input transistors reduces the destructive effect of flicker noise on bio-signals. Substituting the noise generators from (10) and (11) in (9) leads to (12):

$$\overline{i_{n.in}^2} = \frac{4kT}{R_f} + \frac{4kT\gamma}{(gm_n+gm_p)R_f^2} + \frac{K_f}{C_{ox}WLR_f^2} \times \frac{1}{f} + \frac{4kT\gamma}{gm_{(BLRL)}} \quad (12)$$

From (12), it becomes clear that the TIA noise can be reduced by selecting a large value for R_f and (WL) production. It is worth noting that the input-referred current noise of the second stage can be ignored due to the TIA's high gain.

2.1.4. MOS Pseudo-Resistor

According to (8), to achieve a very low frequency (<0.5 Hz) for a high pass corner frequency, the product of C_E R_E must be increased, resulting in an extremely large time constant; Thus, the resistance R_E must have a high value such that f_L is well below 0.5 Hz. Among many different pseudo-resistors, the one presented in [20] and illustrated in Fig. 6 fulfills this requirement. For this complementary pseudo-resistor, the current I_p flowing from source terminal to the drain terminal of M_P operated in subthreshold region can be expressed as:

$$\text{Ip} = I_D(e^{\frac{-V_{BD}+V_{SD}}{V_T}} - e^{\frac{-V_{BD}}{V_T}}) \times e^{\frac{V_{BG}-V_{TH}}{nV_T}} \quad (13)$$

Where I_D in (13) can be given by:

$$I_D = 2n\mu_p C_{ox} V_T^2 (\frac{W}{L}) \quad (14)$$

Where, n, μ_p, C_{ox}, V_T,W and L are subthreshold slope factor, mobility of holes, gate oxide capacitance, thermal voltage, channel width and channel length respectively.

Similarly, the I_n for NMOS device operated in subthreshold region can be expressed as (13) by substituting the mobility of electrons (μ_n)instead of $\mu_p$in (14).

The resistance (R_{xy}) of MOS transistors can be calculated as:

$$R_{xy} = (\frac{\partial V_{xy}}{\partial I_{xy}}) \quad (15)$$

According to (15), corresponding expression for resistance across M_p and M_n can be given by:

$$R_{ax} = (\frac{V_T}{\text{Ip}}) \times (1 - e^{\frac{V_{ax}}{V_T}}) \quad (16)$$

$$R_{bx} = (\frac{V_T}{\text{In}}) \times (1 - e^{\frac{V_{bx}}{V_T}}) \quad (17)$$

The total resistance (R_{ab}) across a and b can be expressed as:

$$R_{ab} = R_{ax} + R_{bx} \quad (18)$$

According to (13), the equivalent resistance depends upon bulk and gate voltages. Therefore, different values of R_{ab}can be obtained by tuning bias voltage at gate terminal of a MOS device.

In the case of complementary pseudo-resistor shown in Fig. 6, by applying suitable value for $VT_{(p)}$ and $VT_{(n)}$, the structure provides the large Tera-ohm resistor. By adjusting the value of voltage tune of $VT_{(p)}$ and $VT_{(n)}$ the value of 1.8Tohm adopted for R_E resistor. We select the $VT_{(p)}$ to be -150mv and VT(n) to be -250mv.

Fig. 7 illustrates R_{ab} versus frequency curve for tunable Pseudo resistor.

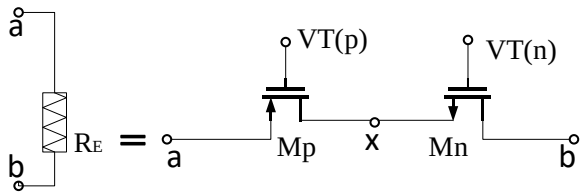


Fig. 6. Pseudo resistor structure for implementing RE[20].

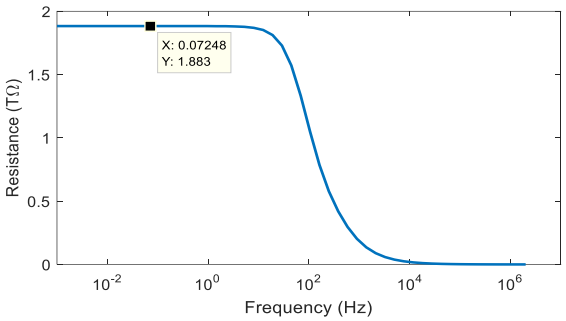


Fig. 7.Resistance versus frequency curve.

3.2. Two-Step Automatic Gain Control (AGC) Loop

Because the PPG sensor can be used in a variety measurement situation, the photocurrent from PD can be a signal with variable-intensity signal. Strong signals can easily cause the high gain TIA to be saturated. To automatically adjust the TIA gain, a two-level AGC loop is added to the circuit. This AGC block is made up of a peak detector, two comparators, and two gain controlling switches, as depicted in Fig. 8.

The AGC block controls the total gain in two steps; the switch of each stage is turned on based on the signal amplitude in the peak detector output. This block detects the TIA output signal's peak and consumes 26.71pW of power. The peak value then compared to two-threshold voltages to generate a control signal for MOSFET switches in the feedback loop. If the peak value exceeds the threshold voltages VTH_1 or VTH_2, the output of the comparators rises and approaches the positive supply rail (V_{DD}), turning on one of the switches SW_1 or SW_2. If the second stage causes the output AC signals to become saturated, the SW_2 control switch turns on, resulting in a larger

feedback capacitor, and lowering the gain of the second stage (fine step). Furthermore, larger input signals would cause the TIA outputs to become saturated; thus, the coarse step gain control is used to reduce the first stage gain, preventing the output signal from becoming saturated. If the output of the peak detector is greater than VTH_2, the comparator's high-level output activates SW_1, resulting in a smaller feedback resistor for the first stage. In our design, the value of VTH_1 is set to 120mV, and the value of VTH_2 is set to 300mV. The R_2 and C_3 are selected to be 1.43MΩ and 1.7 pF, respectively. The schematic of comparators used in this paper is depicted in Fig. 9. With two-level gain-controlling block, the dynamic range of receiver can be increased.

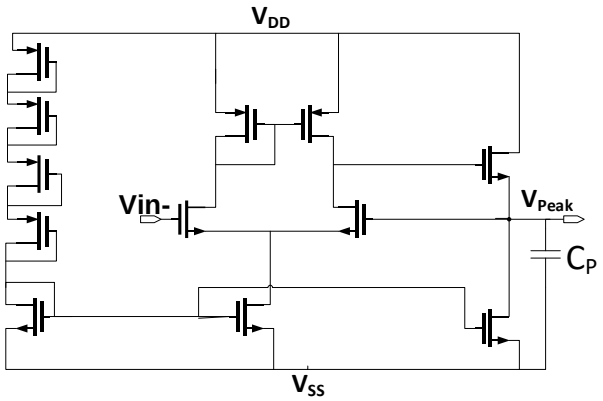


Fig. 8. The circuit of Peak Detector.

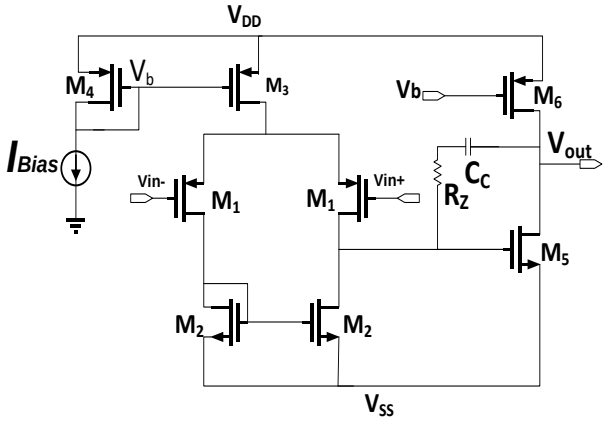


Fig. 9. The circuit of comparator.

3.3. Gm-C Filter Design

The PPG signal's desired bandwidth is 10 Hz. As a result, in the third stage, a low-pass filter is used to remove out-of-band frequency components. A Gm-C filter is implemented in this work to meet the requirements of large resistance and large capacitance in the low cut-off frequency design, as shown in Fig. 10,[21]. The Gm-C filters are suitable choice for low power biomedical applications to tackle the area constraints. The transfer function of a simple Gm-C filter is given by Eq. (19):

$$H(S) = \frac{1}{1+G_m cs} \quad (19)$$

According to (19), instead of using a large capacitor in an area efficient design, designing a transconductor with a low transconductance is a reasonable alternative. The bias current in Fig. 10 is 50nA and the number of parallel and serial transistors is n=20, so the equivalent transconductance is $Gm_0/400$. The equivalent value of Gm in this design is 4.1nS. Table3 summarizes the various performance parameters of the Gm block.

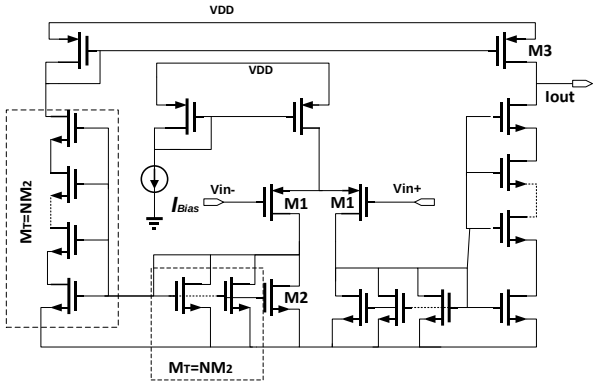


Fig. 10. The schematic of series-parallel OTA as Gm block [21].

Table I. Summary of Gm-block Parameters.

Parameters	Value
VDD (V)	± 0.9
I_B (nA)	50
G_m (nS)	4.1
Power(nW)	127
P.M [Deg]	79
B.W (Hz)	85
Unity Gain Frequency (Hz)	375

4. Simulation result

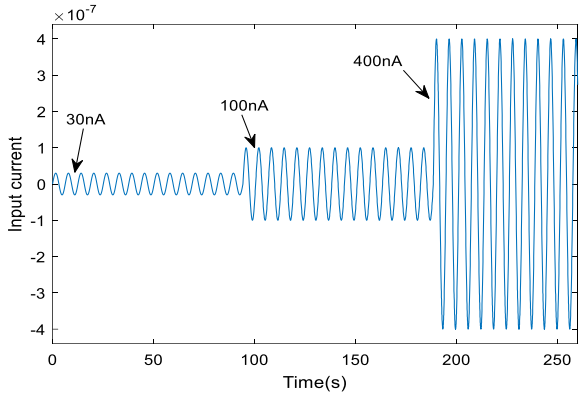
Using Cadence Virtuoso tools, the proposed receiver is designed and simulated in 0.18µm TSMC CMOS process. The circuit design considered the trade-off between gain, noise, and power consumption to meet the requirements for the PPG signal acquisition system.

4.1. AC and Transient Simulation Results

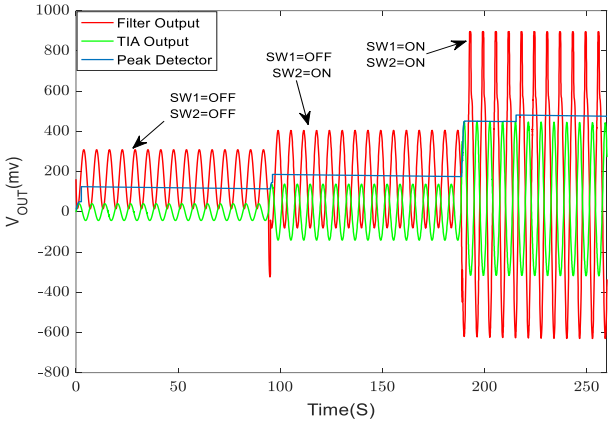
The Post-layout transient response of the entire receiver illustrated in Fig. 11. To evaluate the AGC block response, the input current is applied at three different levels. When the input current is 30nA, neither the TIA stage nor the capacitive feedback stage is saturated, and both the SW_1 and SW_2 switches turned off. The second stage would become saturated if the input current was 100nA. As a result, the SW2 switch is activated to prevent the malicious effect. When the input current is 400nA, both stages become saturated. As a result, both gain controlling switches are activated in this case to prevent both stages from becoming saturated. The AGC block's satisfactory function was confirmed by the post-layout simulation result in Fig. 11.

We also used the PPG signal from the PhysioNet site [22] to assess receiver performance. Fig. 12 depicts the transient response of the receiver following the Gm-C filter block. Fig. 13 depicts the

circuit's AC response. The peak-to-peak amplitude of the input current is 0.1μA, and the DC component of input current ranges from 500nA to 100μA. it is clear from Fig. 12, that the high pass cut-off frequency, F_H varies with I_{DC}. It is worth noting that due to the appearance of the $g_{m(BLRL)}$ term in the numerator of (8), the variations of high pass corner frequency according to input DC current variations is reasonable.



(a)



(b)

Fig. 11. Transient response of TIA. (a) Input current, (b) Peak detector response and output of Gm-c Filter

4.2. Post Layout PVT Simulation Result

The layout of the designed receiver is depicted in Fig. 14, and its area is 0.121mm2. Table 4 summarizes the post-layout simulation results. PVT analysis is used to evaluate the performance of a designed circuit against process, voltage, and temperature (PVT) variation.

Table 5 shows the receiver performance parameter variations across process, voltage, and temperature. Despite ±10% variation of VDD, the receiver maintains high pass cut-off frequency below 0.2 Hz within the temperature range from -25℃ to 40℃ for TT and SS corners; However, for FF state, the low-side temperature is limited to -10℃.

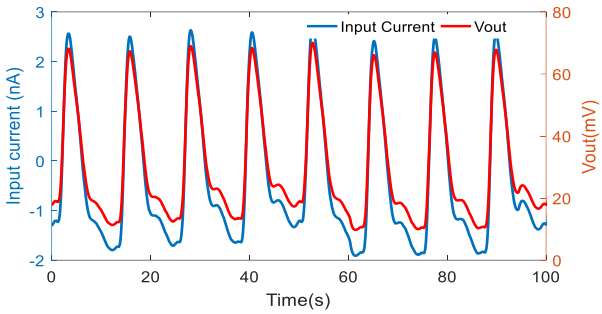


Fig. 12. Transient response of receiver.

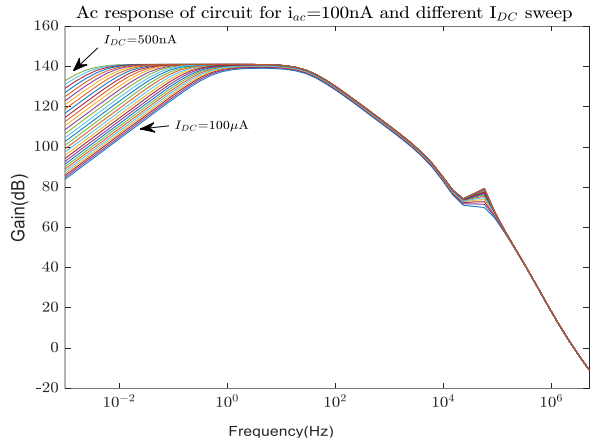


Fig. 13. AC response of receiver for iac=100nA and different IDC, sweep range from IDC=500nA to IDC=100μA.

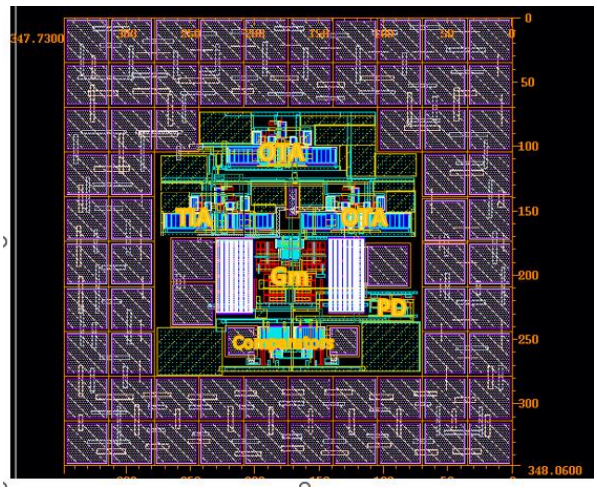


Fig. 14. Layout of PPG receiver.

Table IV. Post-layout simulation performance parameters.

Parameters	Post layout result
Gain(dBΩ)	147.62
Power(μW)	40.14
Input referred noise pArms	39.71
f_L(mHz)	1.2
f_H(Hz)	62.78

4.3. Monte Carlo Simulation Results

The Monte-Carlo simulation for the 1000-run has been done. The computed statistic (mean value ± standard deviation) result of performance parameters is shown in

4.4. Performance Summary and Comparison

Table 6 shows the performance comparison of this design with recent state-of-arts works.

The AFE in[8] has the lowest power of 14.85 µW but it reduces the input-referred noise to only 64.2pArms .

Additionally, the developed chip in [4] consumes a lot of power, reducing battery life. The other works in Table 6 have higher powers and larger areas than the design presented here. The suggested design is frequently regarded as the most affordable solution due to its low power consumption and tiny 0.121 mm2 area. In terms of overall power consumption and noise performance, the proposed design is competitive with current findings.

5. Discussion and Conclusion

This paper presents a receiver for bio-signal recording applications, utilizing a low noise and high gain transimpedance amplifier (TIA). One of the design limitations associated with AFE for PPG sensors is the potential for saturation caused by the high transimpedance gain of the first stage TIA. This saturation risk arises when the significant DC photocurrent resulting from ambient light is not adequately taken care of. The implementation of a BGL cancellation loop in the initial stage serves the purpose of rejecting the DC photocurrent. Furthermore, the second stage incorporates a, two-level automatic gain-controlling scheme, which operates in both fine and coarse steps. This scheme is designed to mitigate any potential distortion that may occur in the PPG signal when the photocurrent reaches high levels.

Moreover, the utilization of PPG AFE is prevalent in scenarios that involve the detection of low-level signals. However, the presence of flicker noise, which is the primary source of noise in circuits operating at low frequencies, poses a challenge in accurately detecting these signals. The mitigation of flicker noise facilitates the detection of signals at lower levels, thereby enhancing the dynamic range. The efficacy of the proposed architecture has been confirmed by post-layout simulations, process, voltage, and temperature (PVT)analysis, as well as statistical analysis. The circuit's ability to effectively reject large input DC components and its performance in reducing noise indicate that the proposed circuit has potential as a suitable choice for acquiring PPG signals.

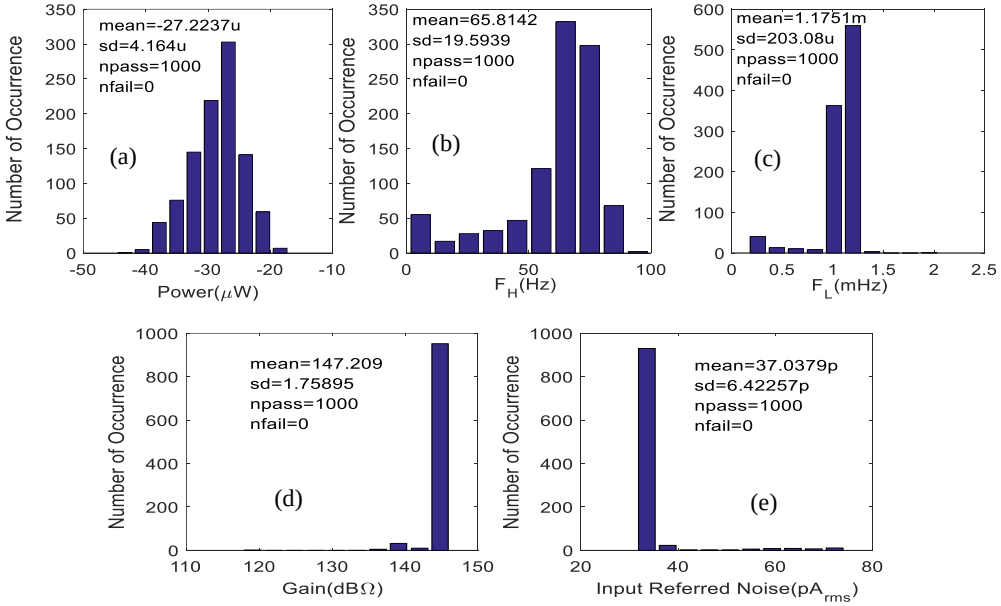


Fig. 15. Histogram of 1000 run Monte-Carlo Simulation. (a) Power, (b)f_H, (c) f_L, (d) Gain, (e) Noise

Table V. Effect of PVT variation on receiver performance parameter.

VDD	±0.9			-10%VDD			+10%VDD		
Process Corner	SS	TT	FF	SS	TT	FF	SS	TT	FF
Temperature[℃]	40	27	-25	40	27	-10	40	27	-25
$Gain(dB)$	148.7	146.5	146.5	148.4	147.3	145.8	148.8	147.7	146.8
Input referred noise(pArms)	34.27	39.36	43.04	34.75	40.63	52.08	36.16	42	42.56
f_L(mHz)	1.157	1.31m	1.53	1.11	1.32	1.68	1.16	1.28	1.54
f_H(Hz)	102.4	120.5	213.7	105.3	127.4	208.6	94.36	107.2	208.8
Power(µW)	32.2	40.32	25.44	11.26	14.22	10.77	77.52	97.36	74.74

Table VI. Performance comparison of the proposed TIA with other published designs.

Ref/Year	Tech (µm)	Area	Power Consumption	Input Noise	Dc Current Rejection	Gain	VDD
[14]/ (2021)	0.35	3.91mm2	50.75 µW	41.3 pArms	24µA	12.5MΩ	3.3V
[8]/ (2019)	0.35	0.64mm2	14.85 µW	64.2 pArms	10µA	142 dBΩ	3.3V
[3]/ (2021)	0.18	2.76 mm2	<100µW	-	-	100 dBΩ	1.8 V
[4]/ (2021)	0.18	3 mm2 (readout +Led driver)	460µW	0.256 nA/√Hz	10µA	>100 dBΩ	1.3-2 V
[5]/ (2008)	0.35	0.67mm2	145µW	40.8 nA/√Hz (30 Hz to 5 kHz)	15µA	63.5 dBΩ	2.5V
This work	0.18	0.121mm2	40.14µW	39.71 pArms	100µA	147 dBΩ	±0.9V

6. References

[1] J. H.-S. Wang, M. H. Yeh, P. C.-P. Chao, T. Y. Tu, Y. H. Kao, and R. Pandey, "A fast digital chip implementing a real-time noise-resistant algorithm for estimating blood pressure using a non-invasive, cuffless PPG sensor," Microsyst. Technol., vol. 26, no. 11, pp. 3501–3516, Nov. 2020, doi: 10.1007/s00542-020-04946-y.

[2] D. H. Nguyen, Y. T. Chen, T. Y. Tu, P. C. P. Chao, Y. W. Fang, and B. S. Lin, "A new blood flow volume sensor with embedded estimation of SpO2 to maximize its accuracy," Microsyst. Technol., vol. 27, no. 6, pp. 2433–2445, 2021, doi: 10.1007/s00542-020-05149-1.

[3] E. F. Pribadi, R. K. Pandey, and P. C.-P. Chao, "Design and implementation of a new light to digital converter for the PPG sensor," Microsyst. Technol., vol. 27, no. 6, pp. 2461–2472, Jun. 2021, doi: 10.1007/s00542-020-05154-4.

[4] R. K. Pandey and P. C.-P. Chao, "An adaptive analog front end for a flexible PPG sensor patch with self-determined motion related DC drift removal," in Proceedings - IEEE International Symposium on Circuits and Systems, May 2021, vol. 2021-May, pp. 1–5, doi: 10.1109/ISCAS51556.2021.9401265.

[5] A. K. Y. Wong, K. P. Pun, Y. T. Zhang, and K. N. Leung, "A low-power CMOS front-end for photoplethysmographic signal acquisition with robust DC photocurrent rejection," IEEE Trans. Biomed. Circuits Syst., vol. 2, no. 4, pp. 280–288, 2008, doi: 10.1109/TBCAS.2008.2003429.

[6] Y. Shu et al., "26.1 A 4.5mm 2 Multimodal Biosensing SoC for PPG, ECG, BIOZ and GSR Acquisition in Consumer Wearable Devices," in 2020 IEEE International Solid- State Circuits Conference - (ISSCC), Feb. 2020, pp. 400–402, doi: 10.1109/ISSCC19947.2020.9063112.

[7] G. Ferrari, F. Gozzini, A. Molari, and M. Sampietro, "Transimpedance Amplifier for High Sensitivity Current Measurements on Nanodevices," IEEE J. Solid-State Circuits, vol. 44, no. 5, pp. 1609–1616, May 2009, doi: 10.1109/JSSC.2009.2016998.

[8] B. Lin, M. Atef, and G. Wang, "14.85 µW Analog Front-End for Photoplethysmography Acquisition with 142-dBΩ Gain and 64.2-pArms Noise," Sensors, vol. 19, no. 3, p. 512, Jan. 2019, doi: 10.3390/s19030512.

[9] A. K. Y. Wong, K. N. Leung, K.-P. Pun, and Y.-T. Zhang, "A 0.5-Hz High-Pass Cutoff Dual-Loop Transimpedance Amplifier for Wearable NIR Sensing Device," IEEE Trans. Circuits Syst. II Express Briefs, vol. 57, no. 7, pp. 531–535, Jul. 2010, doi: 10.1109/TCSII.2010.2048401.

[10] A. Syed, K. Khan, A. Ahmad, M. S. Asad, and W. Saadeh, "A 1mW Vitals Monitoring System for Asthmatic Patients based on Photoplethysmography," in 2019 IEEE Biomedical Circuits and Systems Conference (BioCAS), Oct. 2019, pp. 1–4, doi: 10.1109/BIOCAS.2019.8918724.

[11] H. Zheng, R. Ma, and Z. Zhu, "A linear and wide dynamic range transimpedance amplifier with adaptive gain control technique," Analog Integr. Circuits Signal Process., vol. 90, no. 1, pp. 217–226, Jan. 2017, doi: 10.1007/s10470-016-0867-1.

[12] V. S. Rajan and B. Venkataramani, "Design of low power, programmable low-Gm OTAs and Gm-C filters for biomedical applications," Analog Integr. Circuits Signal Process., vol. 107, no. 2, pp. 389–409, May 2021, doi: 10.1007/s10470-020-01748-0.

[13] B. Lin, M. Atef, and G. Wang, "A low-power high-sensitivity analog front-end for PPG sensor," in 2017 39th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC), Jul. 2017, pp. 861–864, doi: 10.1109/EMBC.2017.8036960.

[14] B. Lin, Z. Ma, M. Atef, L. Ying, and G. Wang, "Low-Power High-Sensitivity Photoplethysmography Sensor for Wearable Health Monitoring System," IEEE Sens. J., vol. 21, no. 14, pp. 16141–16151, Jul. 2021, doi: 10.1109/JSEN.2021.3062189.

[15] K. Puttananjegowda and S. Thomas, "A low-power low-noise multi-stage transimpedance amplifier for amperometric based blood glucose monitoring systems," Analog Integr. Circuits Signal Process., vol. 102, no. 3, pp. 659–666, Mar. 2020, doi: 10.1007/s10470-020-01600-5.

[16] S. Firouz, E. N. Aghdam, and R. Jafarnejad, "A Low Power, Low Noise, Single-Ended to Differential TIA for Ultrasound Imaging Probes," IEEE Trans. Circuits Syst. II Express Briefs, vol. 68, no. 2, pp. 607–611, 2021, doi: 10.1109/TCSII.2020.3018223.

[17] F. Centurelli, A. Fava, G. Scotti, and A. Trifiletti, "80 dB tuning range transimpedance amplifier exploiting the Switched-Resistor approach," AEU - Int.

J. Electron. Commun., vol. 149, p. 154196, May 2022, doi: 10.1016/j.aeue.2022.154196.

[18] A. Atef, M. Atef, E. E. M. Khaled, and M. Abbas, "CMOS Transimpedance Amplifiers for Biomedical Applications: A Comparative Study," IEEE Circuits Syst. Mag., vol. 20, no. 1, pp. 12–31, 2020, doi: 10.1109/MCAS.2019.2961724.

[19] M. Atef and H. Zimmermann, Optoelectronic Circuits in Nanometer CMOS Technology, 1st ed., vol. 55. Springer, Cham, 2016.

[20] K. Sharma, A. Pathania, R. Pandey, J. Madan, and R. Sharma, "MOS based pseudo-resistors exhibiting Tera Ohms of Incremental Resistance for biomedical applications: Analysis and proof of concept," Integration, vol. 76, no. March 2020, pp. 25–39, Jan. 2021, doi: 10.1016/j.vlsi.2020.08.001.

[21] A. Arnaud, R. Fiorelli, and C. Galup-Montoro, "Nanowatt, Sub-nS OTAs, With Sub-10-mV Input Offset, Using Series-Parallel Current Mirrors," IEEE J. Solid-State Circuits, vol. 41, no. 9, pp. 2009–2018, Sep. 2006, doi: 10.1109/JSSC.2006.880606.

[22] A. L. Goldberger et al., "PhysioBank, PhysioToolkit, and PhysioNet," Circulation, vol. 101, no. 23, pp. 215–220, Jun. 2000, doi: 10.1161/01.CIR.101.23.e215.