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A Modified Regulated Cascode transimpedance amplifier with extra feed-forward path to enhance gain and bandwidth

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Abstract
This paper presents a Transimpedance Amplifier (TIA) for high sensitivity Near Infrared Spectroscopy (NIRS). The proposed TIA is based on the Regulated Cascode (RGC) structure with an extra transistor employed to implement additional feed-forward path and achieve higher gain values. The extra transistor senses a partially amplified input signal, available in the conventional circuit, and conveys an additional ac current into the load, which provides a higher gain. In addition, a bandwidth extension method is introduced using a capacitor and resistor, which can improve amplifier's bandwidth by 40%. The proposed TIA is designed in 0.18µm CMOS technology and achieves a transimpedance gain of 101.9dB with a -3dB bandwidth of 91.2 MHz considering 2pF of photodiode capacitance at the TIA input. The input referred noise is 4.4pA/√Hz while dissipating 151µW power.

Keywords
Transimpedance Amplifier, Regulated Cascode, high-gain, bandwidth extension, NIRS.

1. Introduction

Transimpedance amplifiers are widely used in different applications ranging from renowned high-speed optical communication to enhanced healthcare technologies. Specifically, advanced optical devices have been recently utilized for noninvasive medical diagnosis, such as Near Infrared Spectroscopy [1-5]. NIRS emits a laser light signal into the skull or tissue and detects the reflected signal with an optical receiver to evaluate the oxygen. It can be used for monitoring long-term brain activity or regional tissue. NIRS requires a highly sensitive receiver providing bandwidth in the range of Mega Hertz (19M-100M), according to the literature [5].

Like other optical receivers, in NIRS, a large area integrated photodiode (PD) detects the reflected optical power and produces a proportional current. A transimpedance amplifier (TIA) converts the current into voltage and provides amplification of the input signal. TIAs are designed with low input impedance to convey the current to the output efficiently. However, the large photodiode capacitance at the input node creates a dominant pole and limits the bandwidth [6]. Therefore, it is essential to further reduce the TIA input impedance using advanced circuit techniques. This becomes more difficult to achieve when high sensitivity and high speed requirements must be fulfilled.

One typical strategy to achieve low input impedance is the use of a resistive feedback TIA (RF-TIA) [7-10]. In this structure a high gain voltage amplifier employs negative voltage-current feedback through a resistor. The simplest core amplifier could be a single-stage common-source structure. This structure is suitable for high gain and high sensitivity applications since the value of the feedback resistor can be increased despite the limited supply voltage. However, the circuit bandwidth is directly proportional to the feedback resistor, and as the value of this resistor is increased, the bandwidth is reduced. Increasing the open loop gain can be helpful in enhancing the bandwidth. However, it requires higher power consumption.

Regulated Cascode (RGC) amplifier is also a common technique to allow for small input impedances [11-16]. In this structure an active feedback amplifier is used to boost the transconductance of a common-gate current buffer and reduce the input impedance. This structure, was shown to outperform other topologies when ultra-low power consumption and high bandwidth were the primary goal to achieve [5]. However, when higher gain values are required, it would be hard to achieve low input impedances. Hence the bandwidth enhancement is reduced.

In this paper, a modified RGC structure is proposed for NIRS applications that can achieve higher bandwidth at high gain values. In Section 2, the conventional RGC structure is reviewed, and the problem of high gain implementation is explained. The proposed structure is presented and analysed in Section 3 and the simulation results are given in Section4. Conclusion is given in Section 5.

2. Conventional Regulated Cascode structure

The regulated cascode TIA is shown in Fig.1(a), together with its conceptual behaviour in fig.1(b). This structure

consists of a common-gate transistor (M_1) as a current buffer core to convey the photodetector current into the output. Besides, an extra common-source amplifier, denoted as A_1 (consisting of M_2 and R_D), is used as an auxiliary amplifier to boost the transconductance (g_m) of M_1 and reduce the input impedance.The input impedance and gain of this structure can be written as follows:

$$R_{in} = \frac{1}{g_{m1}(1+A_1)} = \frac{1}{g_{m1}(1+g_{m2}R_D)} \quad (1)$$

$$\frac{V_{out}}{I_{in}} = R_L \quad (2)$$

As can be seen, the input impedance is reduced irrespective of the gain. Although the input node is a low resistance one, the high photodiode capacitance would still cause the pole at this node to determine the bandwidth. If the photodiode capacitance would be high compared to the parasitic capacitances, the pole associating the input node would be dominant and can be estimated as follows:

$$\omega_{P,in} = \frac{1}{R_{in} \times C_{PD}} = \frac{g_{m1}(1+g_{m2}R_D)}{C_{PD}} \quad (3)$$

To achieve high gain values, the load resistance must be increased. However, large load resistance requires high voltage headroom which is limited in today's CMOS technology. Hence the bias current of the common-gate branch must be decreased to keep proper voltage drop across the load. Reducing the bias current lowers the g_m of the transistor and increases the input impedance according to (2). Therefore, when RGC structure is designed to achieve higher gain values, the input impedance is increased and bandwidth is reduced. In fact, the gain bandwidth trade-off exists in this structure due to implementation and headroom issues. However, this trade-off cannot be seen in equations (1)-(3). Note that the term $g_{m2}R_D$ is also limited due to the supply voltage and places a limit on input impedance reduction. Therefore, it is not possible to reach higher bandwidths in the traditional RGC circuit even by increasing the power consumption.

3. Proposed structure

To reach higher gain values, a new structure is proposed, as shown in Fig.2(a). As can be seen, a PMOS transistor is added in parallel with the load of the regulated cascode structure with its gate connected to V_x. From one point of view, this transistor acts as a current source parallel with the load and draws part of the dc current provided by M_1. Hence the dc current of the load resistance is reduced. This allows for higher load values while proper voltage drop is kept across the load.

Interestingly, the PMOS transistor increases the gain in a second manner, creating an additional path from input to output. The main path is M_1, which acts as a current buffer and transfers the ac current of the photodiode into output. Additional path, is realized through common-source function of M_2 and M_3. This extra amplification occurs as follows: The input current is converted to the voltage at the input node proportional to the input impedance. Subsequently, M_2 provides an amplification of the input voltage at node V_x. This voltage is sensed by the gate of M_3 and is then converted to current and carried to the load. This is an extra ac current proportional to the input photodiode current and is summed with the photodiode current at the output. A behavioural function of the amplifier is shown in Fig.2(b), where M_3 is demonstrated by its transcoductance, g_{m3}.

Using the conceptual diagram, shown in Fig.2(b), expressions are derived for the input impedance and transimpedance gain as (4) and (5).

$$R_{in} = \frac{1}{g_{m1}(1+A_1)} = \frac{1}{g_{m1}(1+g_{m2}R_D)} \quad (4)$$

$$\frac{V_{out}}{I_{in}} = R_L\left(1+\frac{g_{m3}}{g_{m1}}\frac{A_1}{1+A_1}\right) \xrightarrow{A_1 \gg 1} \approx R_L\left(1+\frac{g_{m3}}{g_{m1}}\right) \quad (5)$$

The input resistance is not changed, while gain is increased by the proportion of g_{m3} over g_{m1}. This confirms the basic idea and function of the circuit.

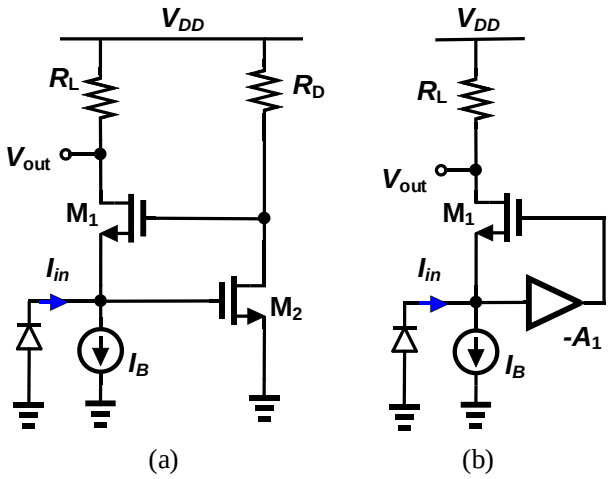


Fig.1. (a) Regulated cascode structure as Transimpedance amplifier (b)conceptual diagram

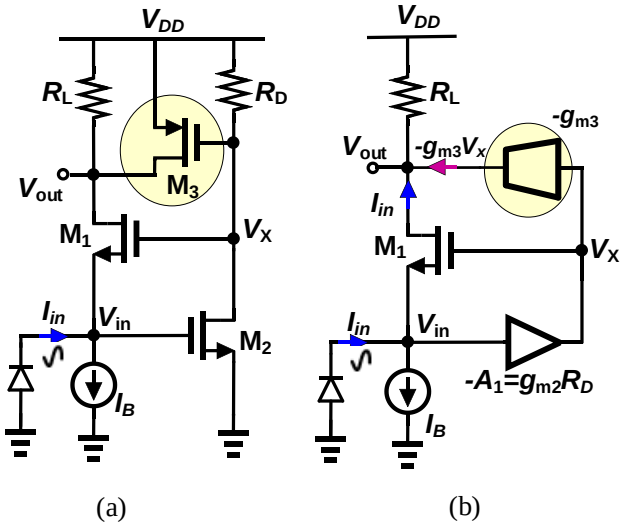


Fig. 2. (a) Proposed Regulated cascode structure with additional feed-forward path (b) conceptual diagram

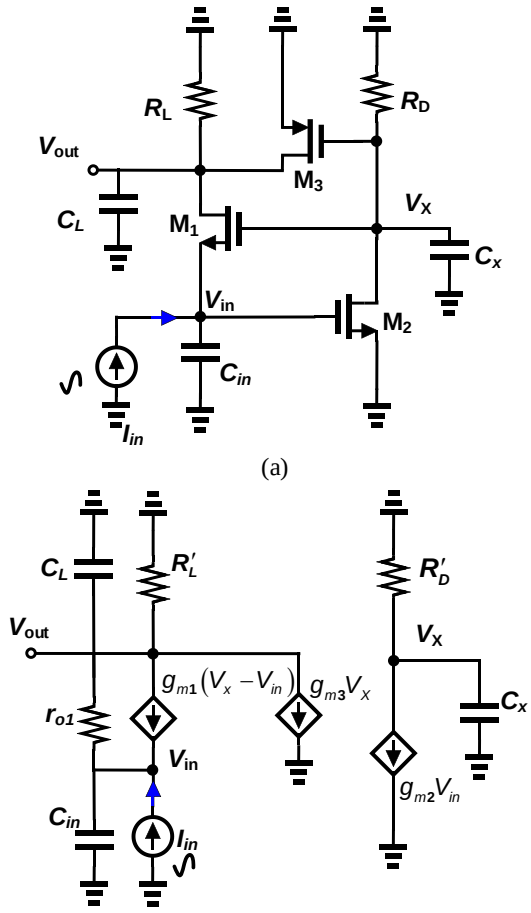


Fig.3. Proposed structure (a) equivalent AC circuit (b)small signal model

3.1. Exact small signal analysis

For exact analysis, however, second-order effects and parasitic capacitances must also be considered. Fig.3(a) shows the Ac equivalent of the proposed circuit together with the parasitic capacitances. Miller effect has been used to simplify the effect of floating capacitances (C_{gd2},C_{gs1},C_{gd3},C_{gd1}) and achieve a circuit where all capacitors are associated from a node to ground. The C_{in} capacitance includes the parasitic capacitances along with the PD capacitance.

Small signal model of the circuit is shown in Fig.3(b), where the output resistances of all transistors are also included. Since the output resistance of M_2 and M_3 appears in parallel with R_D and R_L, respectively, these are easy to consider in the model. Following notations are used to provide conciseness.

$$R'_L = R_L \parallel r_{o3}; R'_D = R_D \parallel r_{o2} \quad (6)$$

Note that the small signal model and derived equations can also be used for the traditional RGC structure considering slight modifications in the values of capacitors. This can be done simply by setting g_{m3}=0 and R'_L=R_L to compare with RGC and setting g_{m3}=0 reveals a situation where gate of M_3 is connected to a to a dc voltage and M_3 acts just as a current source.

Using the small signal model of the proposed structure, the amplifier gain in low frequencies is expressed as:

$$\frac{V_{out}}{I_{in}} = R'_L \times \frac{1+g_{m1}r_{o1}\left(1+g_{m2}R'_D\right)+g_{m3}r_{o1}g_{m2}R'_D}{1+g_{m1}r_{o1}\left(1+g_{m2}R'_D\right)-g_{m2}R'_Dg_{m3}R'_L} \quad (7)$$

If $g_{m2}R'_D$>>1, the transimpedance gain expression can be simplified as follows:

$$\frac{V_{out}}{I_{in}} = R'_L \times \frac{g_{m1}+g_{m3}}{g_{m1}-\frac{g_{m3}R'_L}{r_{o1}}} \quad (8)$$

Setting g_{m3}=0, and employing M_3 as a current source will provide a gain of R'_L. Note that the effective load resistance, R'_L is lower that R_L which can cause a reduction in gain value. However, M_3 can be designed using higher L to provide higher output resistance and supress this effect.

Employing M_3 in the proposed configuration and accounting for the effect of g_{m3}, gain increases by the factor of g_{m3} over g_{m1} (r_{o1} is ignored). This was also predicted in (5) using conceptual diagram of the amplifier.

In addition, including the effect of r_{o1} offers an interesting result of even increased gain because of the negative term that appears in the denominator. This negative term is proportional to g_{m3} and could be quite helpful to compensate the effect of parallel r_{o3}.

To estimate the bandwidth, poles of the circuit must be derived. This can be done by associating a pole to each node. In the designed prototype, very large photodiode capacitance is considered and small transistor sizes causes the parasitic capacitances to be small. Therefore, input node creates a real dominant pole which can be written as follows:

$$\omega_{p1} \approx \frac{1+g_{m1}r_{o1}\left(1+g_{m2}R'_D\right)-g_{m2}R'_Dg_{m3}R'_L}{C_{in}\left(R'_L+r_{o1}\right)} \quad (9)$$

Assuming R'_L to be slighlty lower than R_L, inclusion of M_3 in the circuit in the proposed manner will cause the dominant pole and bandwidth to be smaller. However, as stated earlier, g_{m1} can be increased by increasing M_1 current, which is not possible in traditional RGC structure.

3.2. Proposed Bandwidth extension method

As shown in (8), the low-frequency gain of the amplifier depends on the value of r_{o1} where reducing this resistance will cause the gain to increase. This could be used to introduce a gain-peaking behaviour in the circuit at higher frequencies. The modified circuit is shown in Fig.4(a). As can be seen, a series combination of compensating resistance and capacitance is added in parallel with the drain source of the M_1 transistor. In low frequencies, the C_m capacitor acts as an open circuit and the amplifier gain is the same as (8). While in higher frequencies, the equivalent impedance of the extra branch is reduced, and hence an equivalent lower r_{o1} will contribute in the gain. The lower equivalent r_{o1}, will increase gain in higher frequencies and causes the 3-dB bandwidth to occur farther. The conventional bandwidth extension method, inductive peaking, make use of inductors that occupies area and suffer from low quality factor.

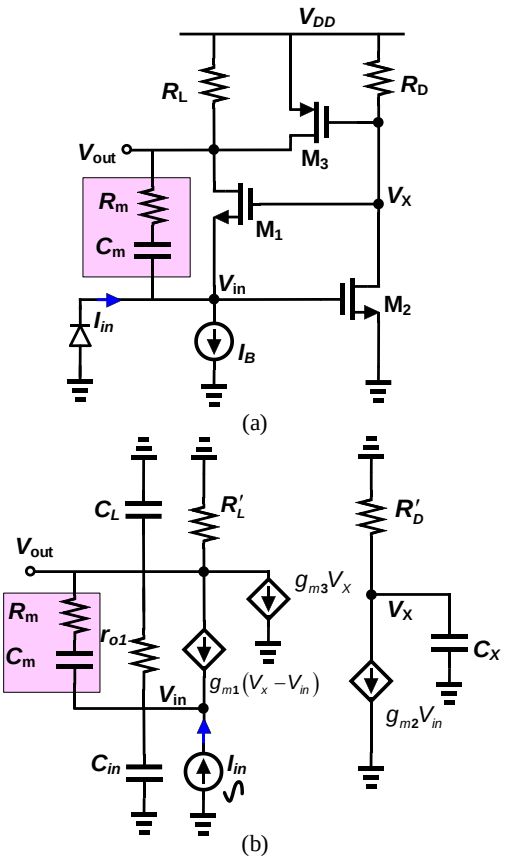


Fig. 4. (a) Proposed bandwidth extension method (b)small signal model

Fig.4(b) shows the small signal model of the circuit. The parasitic capacitances are considered from each node to ground using miller effect. While input and output nodes experience a high capacitance and high resistance respectively, node x has a small capacitance due to parasitics and a moderate resistance. Hence this capacitance, affects the high frequency response and has little effect on determining the bandwidth. To allow for simplicity, C_X is ignored in the following of the paper.

The transfer function of the amplifier is derived as follows:

$$\begin{cases} a_0 = 1+g_{m1}r_{o1}+g_{m2}\left(g_{m1}+g_{m3}\right)r_{o1}R'_D \\ a_1 = C_m\left\{r_{o1}\left(1+g_{m1}R_m\right)+R_m\left(1+g_{m2}\left(g_{m1}+g_{m3}\right)r_{o1}R'_D\right)\right\} \end{cases}$$

$$\begin{cases} b_0 = 1+g_{m1}r_{o1}\left(1+g_{m2}R'_D\right)-g_{m2}g_{m3}R'_DR'_L \\ b_1 \approx C_mg_{m2}r_{o1}R'_D\left(g_{m1}R_m-g_{m3}R'_L\right)+C_LR'_L\left(1+g_{m1}r_{o1}\left(1+g_{m2}R'_D\right)\right)+C_{in}\left(R'_L+r_{o1}\right) \\ b_2 \approx C_mC_Lr_{o1}R'_L\left(1+g_{m1}R_m\left(1+g_{m2}R'_D\right)\right)+C_mC_{in}r_{o1}\left(R'_L+R_m\right)+C_{in}C_Lr_{o1}R'_L \\ b_3 = C_mC_LC_{in}r_{o1}R'_LR_m \end{cases} \quad (11)$$

$$\omega_n = \sqrt{\frac{b_0}{b_2}} \approx \sqrt{\frac{1+g_{m1}r_{o1}\left(1+g_{m2}R'_D\right)-g_{m2}R'_Dg_{m3}R'_L}{C_mC_Lr_{o1}R'_L\left(1+g_{m1}R_m\left(1+g_{m2}R'_D\right)\right)+C_mC_{in}r_{o1}\left(R'_L+R_m\right)+C_{in}C_Lr_{o1}R'_L}}$$

$$\xrightarrow{C_{in}\gg C_m,C_L\,\&\,R'_L\gg R_m} \omega_n \approx \sqrt{\frac{1+g_{m1}r_{o1}\left(1+g_{m2}R'_D\right)-g_{m2}R'_Dg_{m3}R'_L}{C_{in}\left(C_m+C_L\right)r_{o1}R'_L}} \quad (12)$$

$$\frac{V_{out}}{I_{in}} = R'_L \times \frac{a_0+a_1s}{b_0+b_1s+b_2s^2+b_3s^3} \quad (10)$$

Where a_0-a_1 and b_0-b_3 are expressed in (11), considering $r_{o1} \gg R_m$.

The transfer function has a real pole and a pair of complex conjugate poles which is formed due to the coupling path between the input and output nodes. With the help of simulation results, it was found that conjugate poles are dominant and determine the bandwidth and the real pole is located farther. To provide an estimate for the dominant complex poles, the denominator can be approximated with a second-order polynomial and the natural frequency of the poles can be calculated considering b_0-b_2 only (see (12)).

The natural frequency is a function of C_m and C_L in addition to the photodiode capacitance. Therefore, C_m can be chosen to reach the desired bandwidth. However, care must be taken for choosing C_m value. Increasing this capacitance will reduce the b_1 coefficient and increase the quality factor of the poles which increase peaking in the frequency response. Besides, large C_m values might cause b_1 coefficient to be negative, and the complex poles will move to the right half plane. In addition, R_m has no effect on the natural frequency assuming $R_m \ll R'_L$. More intuitive analysis will be given in the next section to show the effect of C_m on the frequency response and choose proper design parameters. Assuming that the third pole is real and located far from the origin,it can be approximated as follows:

$$\omega_{p3} = \frac{b_2}{b_3}$$

$$\omega_{p3} \approx \frac{g_{m1}\left(1+g_{m2}R'_D\right)}{C_{in}}+\frac{\left(R'_L+R_m\right)}{C_LR'_LR_m}+\frac{1}{C_mR_m} \quad (13)$$

$$\xrightarrow{C_{in}\gg C_L,R_m\ll R'_L} \omega_{p3} \approx \frac{1}{R_m}\left(\frac{1}{C_L}+\frac{1}{C_m}\right)$$

As shown in (13), the real pole is determined by C_m and C_L which are considered to be small compared to the large PD capacitance. Besides, R_m is assumed to be a small value compared to R_L Therefore, the third pole is located in high frequencies and has no effect in the bandwidth. This analysis confirms the assumption of dominant complex pole and a far real pole.

In addition,the transfer function has a zero which is introduced because of the additional path created by C_m and R_m and can be approximated as follows:

$$\omega_z = \frac{a_0}{a_1} \approx \frac{1}{R_m C_m} \tag{14}$$

The zero is located at high frequencies above the 3-dB bandwidth.

3.3. *noise performance*

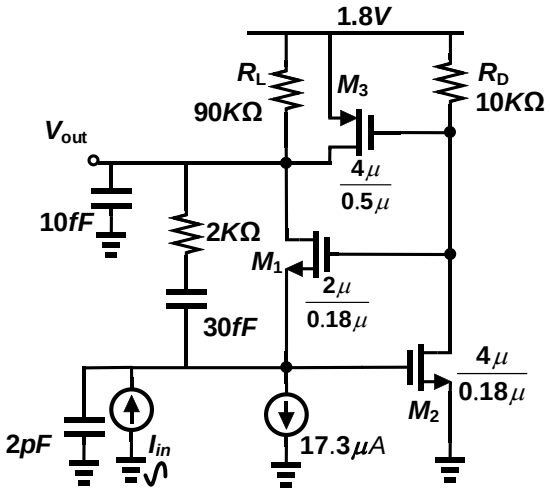
Noise performance of the circuit must also be considered. Since M_3 is added to the output node, its current noise is introduced to the output. In addition, inclusion of M_3 modifies the noise transfer function of other elements. The input referred noise can be written as follows, assuming $r_{o1}=\infty$ and $g_{m2}R_D>>1$:

$$\begin{aligned}\overline{I_{n,in}^2} = &\left\{\overline{I_{n,M_2}^2} + \overline{I_{n,R_D}^2}\right\}\left(\frac{g_{m1}g_{m3}}{g_{m1}g_{m2}+g_{m2}g_{m3}}\right)^2 \\ &+\left\{\overline{I_{n,R_L}^2} + \overline{I_{n,M_3}^2}\right\}\left(\frac{g_{m1}}{g_{m1}+g_{m3}}\right)^2 \\ &+\overline{I_{n,M_B}^2} \\ &+\left\{\overline{I_{n,M_1}^2}\right\}\left(\frac{g_{m3}}{g_{m1}+g_{m3}}\right)^2\end{aligned} \tag{15}$$

Note that the ideal dc current source, shown in Fig. 4(a), is implemented with a transistor and I_{n,M_B} denotes the noise current of the bias transistor. As can be seen noise current of the extra transistor, M_3 appears in addition to the M_1, M_2 and R_D contributions. Besides, M_1, M_2 and R_D transfer functions are proportional to g_{m3} which shows that they contribute to the input noise because of the addition of M_3. Hence, we expect increased noise current in the proposed structure compared with the RGC one. However, noise contribution of R_L is reduced in the proposed structure. This can be seen by inspecting (15) in more details. By setting g_{m3}=0 the term associated with noise of R_L is simplified to unity. i.e the input referred noise is $\overline{I_{n,in}^2} = \overline{I_{n,R_L}^2}$ which shows that the noise of the load is directly referred to the input. However if $g_{m3}\neq 0$ the noise is reduced due to $\overline{I_{n,in}^2} = \overline{I_{n,R_L}^2}\left(\frac{g_{m1}}{g_{m1}+g_{m3}}\right)^2$. This is a result of employing M_3 in the amplification path rather than just acting as a current source parallel with load.

4. Circuit design and verification

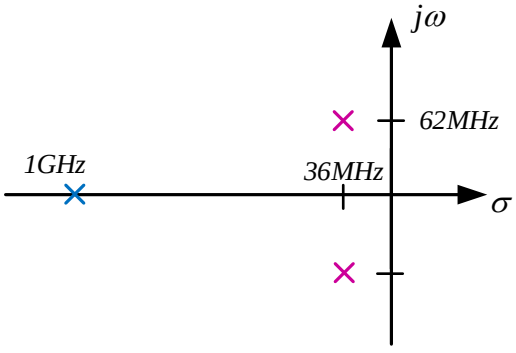
The proposed TIA is designed in 0.18μm TSMC CMOS process and supply voltage of 1.8V. A 2pF photodiode capacitance and 10fF load capacitance are considered for the circuit. The load capacitance is used to model the effect of next stage, and the choice of the PD capacitance is based on [5], where a relatively small PD capacitance is considered to be reasonable for NIRS application. Fig.5 shows the implemented circuit with its small-signal parameter values and pole location derived by pole-zero analysis.



(a)

Transistor parameter	Value (A/V)	Transistor parameter	Value (Ω)
g_{m1}	268µ	r_{o1}	152K
g_{m2}	853µ	r_{o2}	55K
g_{m3}	98.7µ	r_{o3}	666K

(b)



(c)

Fig.5. (a) implemented proposed circuit (b) small-signal parameter values and (c) pole location derived by pole-zero analysis.

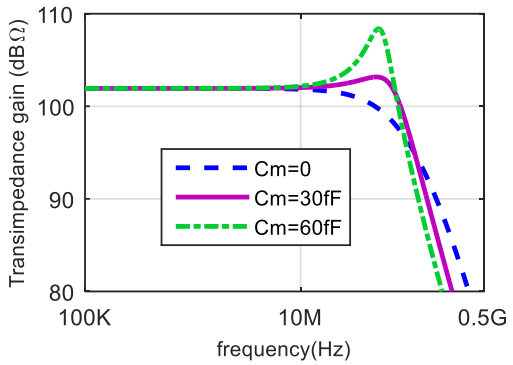


Fig.6. frequency response of the proposed circuit by varying C_m value

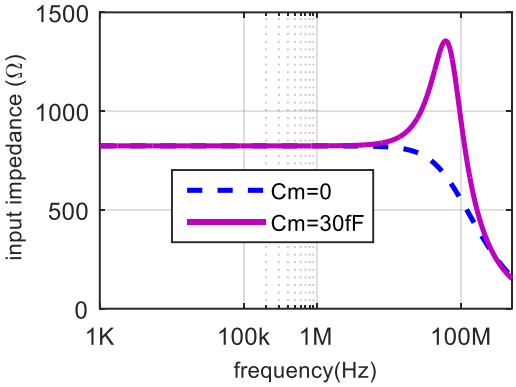
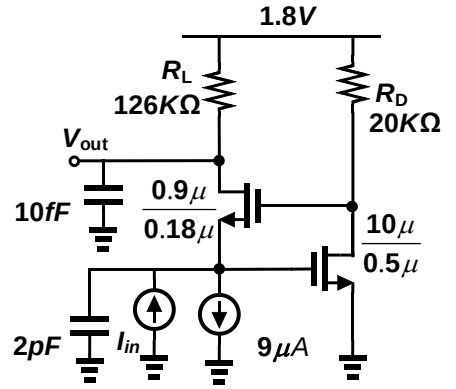
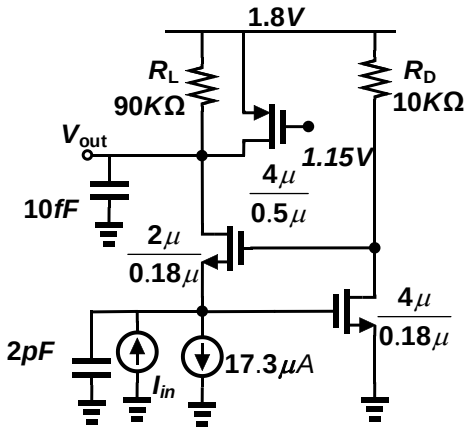


Fig. 7. input impedance of the proposed circuit with and without bandwidth extension



(a)



(b)

Fig.8. Circuit Schematic of TIAs for comparison (a)Reference TIA1 (b) Reference TIA2

The value of R_L is considered lower than the required gain and bias current is chosen based on headroom limitation and input impedance requirements. M_3 is designed to provide portion of the bias current. All transistors are designed with minimum Length except for M_3 where its channel length modulation is quite effective in the circuit performance. To choose proper values for R_m and C_m simulations are carried. The value of C_m has a significant effect on the frequency response. Fig.6 shows the frequency response of the proposed circuit by varying C_m value from 0 to 60fF. The amplifier achieves a gain of 101.9dBΩ in all cases. The bandwidth of the amplifier is 64.7MHz when no compensating branch is used. While for a 30fF C_m value the frequency response experiences a peaking of 1.3dB and reaches a bandwidth of 91.2MHz. It also provides sharper roll-off, which reduces the effect of out-of-band noise. For 60fF C_m value, the poles are moved toward the origin and hence a peaking of 6dB occurs while bandwidth is also reduced. Therefore, a value of 30fF capacitance is considered for C_m. By increasing R_m, however, the bandwidth is changed to a small amount. Where for an increase of R_m up to five times the initial 2kΩ, the bandwidth is reduced by only 5%.

The input impedance of the amplifier is also shown for the two cases of C_m =0 and C_m =30fF. As shown in Fig.7, the input impedance presents an inductive behaviour when the compensating branch is added.

To verify the effectiveness of the proposed structure, a traditional RGC structure is also designed for the same gain and optimized to achieve maximum bandwidth. Besides, a second scheme is considered for comparison where the gate of the additional transistor is connected to a constant voltage and acts as a current source. These structures are called reference TIA1 and 2, respectively. Circuit schematics together with design parameters are shown in Fig.8. Similar photodiode capacitance and load capacitance are considered for the circuits.

The frequency response of the three structures is plotted together and shown in Fig.9. The proposed circuit and Reference TIA1 achieve the same gain of 101.9dBΩ, while the reference TIA1 has a bandwidth of 23.4MHz. This bandwidth is increased to 91.2MHz by the proposed technique. Worth noting that the proposed structure makes use of a lower R_L as the load resistance compared to the RGC, which would reduce the circuit area as well. On the other hand, connecting the gate of the PMOS transistor to a constant voltage as the Reference TIA2 reduces the gain to 98.2dBΩ. This value is lower than the ideal R_L value (81.2K instead of 90K) and is due to the parallel effect of r_{o3}. This effect also exists in the proposed structure, but it is reduced due to the feedback mechanism of r_{o1} resistance and is discussed earlier in this paper. Hence connecting the gate of the PMOS transistor to the drain of M_2 and amplifying a signal rather than just acting as a current source, proves useful in terms of reaching higher gain values while no extra power is required. The Reference TIA2 achieves a bandwidth of 69.9MHz, which is higher than reference TIA1 and results from higher power consumption. These structures are compared in terms of Figure of Merit (FOM) in the following of the paper.

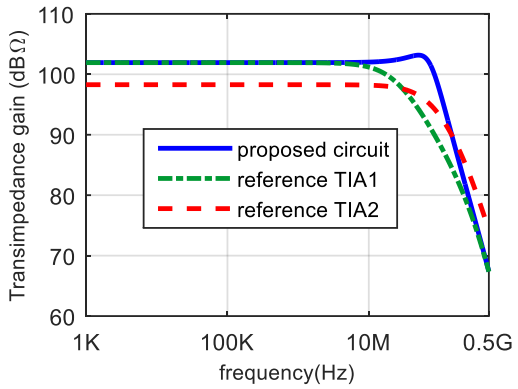


Fig.9. Frequency response of the proposed TIA and reference TIAs.

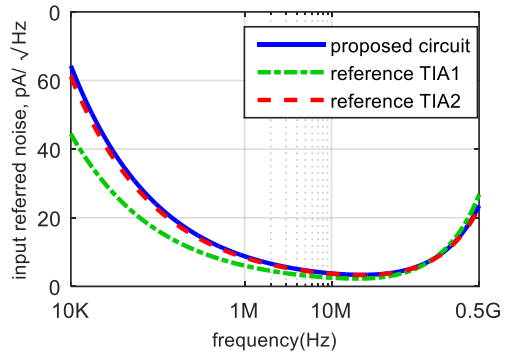


Fig. 10. Input referred noise current power spectral density for the proposed TIA and reference TIAs

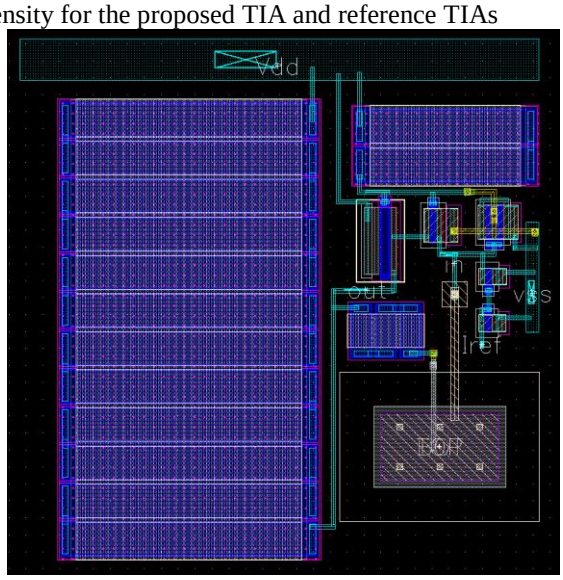


Fig. 11. Layout of the proposed TIA

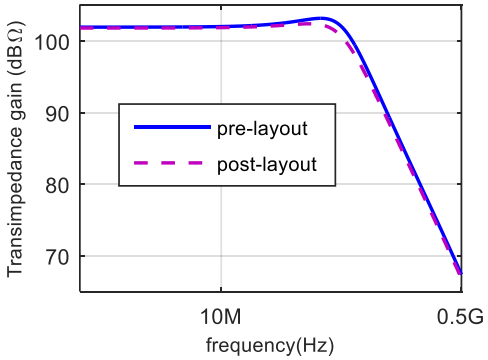


Fig. 12. Pre and Post layout simulation results of the frequency response

Input referred noise of the amplifier is shown in Fig.10. As was predicted, the noise floor is slightly increased in the proposed structure compared with the traditional RGC. However, the noise is almost the same when compared with reference TIA2. Note that inserting a PMOS transistor as a current source to draw current is a well-known technique for increasing the gain. Nonetheless, the noise of the transistor is directly added to that of R_L and the input referred noise is increased when long channel transistors are utilized [6]. Hence, it is inevitable to tolerate a little bit of increased noise in the proposed structure as well as reference TIA2. In comparison, the proposed circuit provides other advantages than reference TIA2. It is worth mentioning that in the proposed circuit, the noise contribution of the resistor R_m is relatively small and is less than 0.0025% of the total integrated noise current.

Table I summarizes the performance of the proposed TIA, reference TIA 1,2 and other state-of-the-art high-gain TIAs achieving bandwidth in the range of MHz. The average input noise current was calculated by integrating the input noise up to the 3-dB bandwidth and dividing the rms noise current by the root of the bandwidth.

To allow for fair comparison, structures with very high power consumption are not included in the table. However, [5] reviews various TIA architectures and provides a good comparison between different topologies. For a bandwidth of 100MHz dedicated for NIRS application, Regulated cascode, Inverter cascode and Regulated Inverter cascode (RIC) architectures proved to show the best performance among other topologies. FOM presented in [20] is used to compare different structures

$$FOM = \frac{Gain(K\Omega)\times Bandwidth(GHz)\times C_{PD}(pF)}{input\ noise\left(pA/\sqrt{Hz}\right)\times power(mW)} \quad (16)$$

As can be seen, our analysis also confirms the superiority of the RGC structure, where it demonstrates a high FOM compared to others. Besides, adding the PMOS transistor as in Reference TIA2 configuration, just to draw current, leads to lower FOM. While additional power results in increased bandwidth, the noise level increases further and deteriorates the FOM as was predicted.

On the other hand, the proposed architecture achieves a higher FOM than the current drawing scheme and the conventional RGC structure. It increases bandwidth up to 400% which was impossible to realize using the conventional RGC topology considering the limited voltage supply.

Layout of the proposed circuit is shown in Fig. 11. The circuit occupies 961µm^2 of silicon die area. To consider the effect of resistance and capacitance in the process, post-layout simulations are carried. Fig. 12 depicts the results of pre and post layout simulations which shows that the parasitic effects do not change the performance of the proposed TIA, dramatically. As shown, in post- layout simulation bandwidth is reduced to 83MHz which shows less than 10% reduction compared to pre-layout simulations.

Table I. Performance summary of the proposed TIA, reference TIAs and other reported high-gain TIAs

	[4]*	[5]*			[17]	[18]	[19]	This Work*		
		RGC	Inv Cascode	RIC				Reference TIA1	Reference TIA2	Proposed structure
Technology	0.13µm CMOS	0.13µm CMOS			0.18µm BCDMOS	0.18µm CMOS	0.11µm CMOS	0.18µm CMOS		
Supply (V)	1.2	1.2	1.2	1.2	±0.9	3.3	1.8	1.8	1.8	1.8
C_{PD} (pF)	2	2	2	2	15	2	2.4	2	2	2
Gain(dBΩ)	104.8	85	95.6	96.3	107	106	87.6	101.9	98.2	101.9
Bandwidth (MHz)	50	100	100	100	7	50	350	23.4	69.9	91.2
Input referred noise(pA/√Hz)	2.2	4.1	2.2	2.46	1.7	1.52	3.67**	3.58	4.3	4.4
Power (mW)	0.34	0.1	0.57	0.57	5.2	8	15.66	0.076	0.151	0.151
FOM	23.23	8.63	9.6	9.3	2.66	1.64	0.35	21.4	17.5	34.1

* simulated

** noise of the complete receiver

5. Conclusion

A modified RGC transimpedance amplifier is proposed which can substantially improve the gain bandwidth performance. The proposed configuration increases the gain of the amplifier by employing an additional feed-forward path and could achieve higher bandwidth at high gain values. Besides, an inductor-less bandwidth extension mechanism is introduced which can increase the bandwidth without increase in noise and power consumption. The proposed structure was validated in 0.18µm CMOS technology and achieved 91.2MHz bandwidth and 101.9dBΩ gain in the presence of a 2pF photodiode capacitance while consuming 151µW of power.

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