Assessing a Noise Reduction Method for a Low-Noise Amplifier

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Abstract
With regards to wireless receiver systems, the effects of noise from all the following phases can be reduced using the gain of the low-noise amplifier (LNA). Therefore, boosting the specified signal power without adding a lot of noise and distortion will be necessary for the signal to be retrievable in the later phases or stages of the system. The proposed method in this study for noise reduction is based on the combination of two techniques: reversed- phase noise signal and non-reversed phase signal. The theoretical model for noise cancellation is presented along with the equations for the overall noise value, which are derived based on a two-port model. The circuit design is implemented using the $TSMC$ 0.18 μm $CMOSRF$ technology on a Cadence Spectre RF tool. The current study also implemented a CMOS UWB LNA configuration with inter-stage matching as well as shunt-series inductive peaking. This design uses inductive source degeneration cascode technology along with an inter-stage matching network. Moreover, to boost impedance matching and power gain, a Chebyshev band pass filter is placed at the input while a shunt-series inductive peaking is placed at the output.

Keywords
Noise, CG UWB LNA, CMOS RF technology.

1. Introduction

With regards to wireless receiver systems, the effects of the noise from all the next stages or phases can be reduced by the gain from the LNA, while its noise is directly injected into the receiver. Therefore, it is required to increase the specified signal power without significantly increasing the potential noise and distortion for the signal to be retrievable in the later phases of the system. The most recent studies use LNAs with a range of a few MHz to 10 GHz inside the wireless receivers which utilize a single LNA for processing of the adjacent broadband signal. There are several strategies for creating narrow-band and wide-band LNAs that use a basic common source and gate configurations with a small number of improvements. LNAs using common source configuration along with inductive degeneration can provide acceptable input matching for the wide-band. Nevertheless, these require a passive network at the input phase which requires a large number of high Q inductors. Furthermore, LNAs using this configuration is capable of providing good noise performance for narrow-band (NB) applications; however, they are not suitable for corner frequencies in wide-band applications.

Recent studies have shown that LNAs from a few MHz to 10 GHz can be used inside wireless receivers which utilize a single LNA for the processing of the adjacent broadband signal. Moreover, there are different strategies for designing narrow-band and wide-band LNAs; these include using the basic common source and common gate configurations using several boosting techniques such as using methods for cancelling noise.

One of the most common architectures for designing the integrated CMOS RF circuit and the microwave circuit involves inductive source degeneration using a cascade (The cascode is a two-stage amplifier that consists of a common-emitter stage feeding into a common-base stage) transistor LNA [1]. In this type of LNA, the cascode transistor is capable of mitigating the miller effect and boosting reverse isolation. In the design of the LNA, the virtual gate- drain capacitance of the first phase or stage; namely miller capacitance defined as, $C_M = C_{gd}(1 + A_{v1})$, will limit the high- frequency bandwidth to $1/RC_M$, where C_M will be amplified by its own gain (A_{v1}). Thus the effective or Miller capacitance C_M is the physical C_{gd} multiplied by the factor. Therefore, the cascode transistor using this capacitance is capable of

protecting the direct shorting of the input and output. Furthermore, to increase the isolation between the two phases or stages of the system, an inductor can be used [2]. This inter-stage inductor can reduce the input impedance of the second stage, which will increase the current pump towards the output [3]. The current study utilizes a UWB LNA design which makes use of an inter-stage matching network to hold the desired signal forward through stopping any unsought signal. Moreover, the design also utilizes a Chebyshev band pass filter to match the input, while it uses a shunt-series inductive peaking network at the output in order to increase the power of the desired signal. The simulation study is carried out using the TSMC 0.18 μm CMOS technology on a Cadence Spectre RF tool.

The current paper tries to design and implement a low-noise CMOS amplifier for wireless receivers in order to reduce the thermal noise and improve the gain. The study first discusses different available design topologies for narrow-band, wide-band, and noise cancelling low-noise amplifiers in detail. Later, the study focuses on a common source amplifier with resistive and inductive loads, cascode configurations, and resistive feedback configurations. Moreover, with regards to broadband applications, amplifiers of the following types are discussed: common gate, distributed, and LC-filter. Furthermore, several noise cancelling LNAs including feed-forward amplifiers, common gate- common source amplifiers, and inductor-less cross-coupled amplifiers will be discussed. The study shows that strategies for cancelling noise sometimes neglect to consider gain improvement.

In the circuits of low-noise amplifiers, there are a number of active and passive parts, which may increase the thermal noise in the LNA. The amount of the increase in the thermal noise by these parts depends on the frequency of operation. Therefore, exploring and evaluating the main sources of noise are carried out in a three-stage common-gate low-noise amplifier. Later on, a new method for cancelling noise is proposed and its theoretical analysis is presented. This new method of noise cancellation can reduce a major portion of the thermal noise. A complete design for the LNA with the proposed method for noise cancellation is implemented, and it reduces the noise while at the same time increasing the gain.

Furthermore, a boosted LC-filter amplifier design is applied for the UWB range. In order to match the input impedance in the frequency range of 3.1 GHz to 10.6 GHz, using a filter design tool, a Chebyshev band-pass filter was designed and implemented on Cadence. In addition, an inter-stage passive network is added in order to send more current towards the input based on the desired frequency range and to bypass the undesired frequency band signals. Therefore, the LNA designed here utilizes shunt-series inductive peaking as well as inter-stage matching. Later in the study, theoretical analysis using small- signal equivalent models for matching the impedance of the input, inter-stage matching, and shunt-series inductive peaking is presented along with models for gain and noise as well as the equations obtained for different stages. The topology of the design presented here is an inductive source degeneration cascode topology equipped with an inter-stage matching network, which provides better matching for the input impedance as well as a better gain.

1.1. Narrow-Band and Wide-Band Design Strategies

Some basic design configurations for LNAs (low noise amplifiers) have been accepted that may be able to meet the minimum performance level; however, these have several deficits. The first design which can be a simple basic LNA configuration is the common source amplifier which uses a resistive load. Nevertheless, this design cannot provide accurate matching for the impedance, and another problem with this design is that the time constant (RC) at the output prevents operation under high frequencies. Furthermore, the resistive load required additional DC voltage. In contrast, the common source amplifier using the inductive load required a lower amount of DC voltage. Also, at the output node, the inductive load resonates with total capacitance, enabling operation at higher frequencies than the former design configuration. Nevertheless, because of significant parasitic capacitances and lack of sufficient isolation between the input and output nodes, this configuration cannot provide a high level of performance. Therefore, this design is rarely used in RF design. On the other hand, the cascode common source amplifier using inductive degeneration offers isolation between the input and output nodes and separates the inductive load from the input resistance. Another way to design the common source amplifier is to use resistive feedback. In this configuration, the feedback resistance (R_f) measures the voltage at the output node and returns a current to the input node. This design configuration is free from the instant tradeoff for the gain and it has no bias current while providing a flat gain of $Av = \frac{1}{2}(1 - R_f/R_s)$. Furthermore, this configuration enables acceptable wideband input matching and since $Z_{in} = 1/g_m$, if $g_m = 20\ mS$, then $Z_{in} = 50\ \Omega$. The estimated noise value for this configuration, i.e.$(1 + \gamma + \gamma g_m R_s)$, indicates that the value of the noise is higher than 3 dB. Where R_S is the resistor, $g_m$is upon multiplication and Z_{in} is passive RLC. Nevertheless, this configuration can be used if the operation frequency is lower than the f_T of the junction transistor.

There have been a number of configurations that utilize noise cancellation methods. For instance, a method for cancellation of thermal noise utilizing resistive feed-forward CS (Common-source) configuration was used for an LNA operating below 2 GHz [4-7]. Later on, using inductive peaking, this configuration was used for higher frequencies, resulting in a reduction in the amount of noise in the frequency range of 3.1 GHz to 10.6 GHz [8]. Moreover, a number of distinct noise cancellation methods have been proposed in previous studies [9-14]; these include a method for simultaneously cancelling noise and third-order distortion in a CG-CS (Common-

gate common-source) cascode LNA operating at the frequency of 2.1 GHz [9, 10], as well as the method using resistive feed- forward for noise reduction in a two-stage differential transconductance LNA operating at a frequency of 4.5 GHz [11]. However, these methods for the cancellation of noise neglect gain improvement [15-19].

Bisht and Qureshi [20] proposed a low-power, low-bandwidth low-power amplifier (LNA) for the GSM band, DCS-1800 and 802.11b/g. Increased gain, low noise, and dual-band performance were obtained using a gain-enhancing technique using transformer-coupled feedback, and positive feedback was obtained using a source tracker. The simulation results showed that the reliability of the LNA was from 1.86 GHz to 2.4 GHz. Han et al. [21]. Low Sound Amplifier (LNA) Low Sound Amplifier (LNA) 100 MHz to 6 GHz Broadband Amplifier provided a single differential for multi-standard radio programs. Two mechanisms of noise removal techniques were introduced in this work. A progressive thermal noise cancellation technique was used in the design of the inverted amplifier to increase the conductivity to achieve the adaptation of broadband input, high gain, and low noise form at the same time. Also, the balanced balloon function converts the thermal noise of the common gate transistor into a common state signal and cancels it at the LNA differential outputs. The proposed design is based on a standard 0.18-um RF CMOS technology and occupies a mold area of 0.04 mm^2. Chaghaei et al. introduced an anchorless and differential bandwidth LNA, which used a complementary current reuse structure and an active and passive amplification technique, which resulted in increased voltage, reduced power consumption, and noise in the signal reception path. Thus, the proposed LNA was able to achieve a bandwidth of 50 MHz - 1.7 GHz with less than -14.26 dB, maximum voltage increase of 20.2 dB, minimum NF 3.31 dB [22, 23].

2. Methods

2.1. A Novel Noise Cancellation Method for CG UWB LNAs

In this part of the study, a new design for the common-gate low-noise amplifier (LNA) is presented that utilizes a completely new method for noise cancellation, which reduces the noise while increasing the gain. In this section, the main thermal noise source is cancelled using an input matching device, and the theoretical analysis will also be presented. Significant reduction of the level of noise (NF) is proved using this new method.

The study presents a design for a common-gate LNA utilizing a noise cancelling method that reduces the noise while boosting the gain. The study also analyzes the noise contributions from the active and passive parts of the CG LNA according to [24]. The input matching device in the first CG transistor is the main source of noise in the system. The proposed method combines two paths. The first path is based on a reversed-phase noise signal while the second is based on a non-reversed-phase noise signal. However, the RF signals along both paths will be in-phase. These two paths were designed based on a symmetrical cascade combination of CG-CS and CS-CG stages. We will present the theoretical model for the total value of noise as well as the equations derived for the total noise figure. The simulation is done utilizing the TSMC 0.18 μm CMOSRF technology on a Cadence Spectre RF tool.

The noise cancellation circuit is designed in a way to cancel the noise generated by M1. Fig. 1 depicts the proposed noise cancellation method in its simplified form, where $\bar{I}_{n,M_1}^2$ is the channel noise generated thermally with a current of $4kT\gamma g_{m1}\Delta f$. The equivalent noise voltage, $\bar{V}_{n,M_1}^2$ at the M1 gate, is equal to $4kT\gamma\Delta f/g_{m1}$. There is a phase shift equal to 180° in the noise voltage at node B and gate M1 caused by the CS stage (the source for M1 is the common terminal), while it is in-phase at node A caused by the next stage (the drain for M1 is the common terminal). Hence, the noise voltages at node A and node B become 180° out of phase. Afterward, there is another 180° phase shift between the noise voltage of node A and node C, caused by the CS stage, so the noise voltages at nodes B and C are in-phase. This CS amplifier (M2) also amplified the RF input signal, V_s.

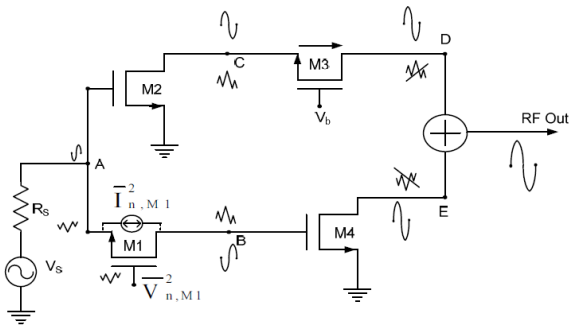

Fig. 1. The Concept for Noise Cancellation in the LNA.

It is shown that the noise voltage of M1 is in-phase at nodes C and D due to the CG stage (M3). However, the noise voltage at node E is 180° out of phase with the related noise voltage at node B, which is due to the CS stage (M4). This ultimately causes the noise voltages at nodes D and E to be 180° out of phase; however, by adding them at the output, these are cancelled. In the meantime, the RF input signal is amplified through paths A-C-D and A-B-E, so the phase shifts of these two paths are identical. Moreover, the amplified RF signals at nodes D and E are in-phase, so they are added at the output node using the associate adder circuit. So it can be concluded that this configuration amplifies the RF input signal while cancelling the noise from the source of the main thermally generated noise.

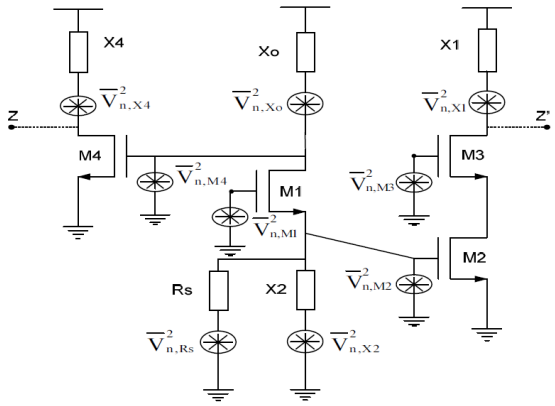

Fig. 2. The Main Sources of Noise in the LNA.

Fig. 2 depicts the sources of noise in the first two stages of the design. The theoretical values for noise voltages of transistors and resistors are $4kT\gamma\Delta f/g_{mi}$ and $4kTR_i$, respectively, where k is the Boltzmann constant, T is the absolute temperature, γ is the transistor parameter, g_{mi} is the transconductance of the i^{th} transistor, and R_i and X_i are the equivalent resistor and impedance for the i^{th} inductor. In the analysis presented below, we assume that the noise of $M1$ is cancelled and the remaining elements of the first two stages of the design are contributing to the total noise value.

If we assume that F_z and $F_{z\prime}$ are the noise factors are two distinct output nodes of z and z', depicted in Fig. 2, then equations 3, 4, and 6 are obtained for F_z and $F_{z\prime}$. Moreover, the noise factors from the first two stages are significantly contributing to the total value of noise.

$$F_z = 1 + \frac{noise\ power\ at\ node\ z\ created\ by\ R_0,R_2,R_4,and\ M_4}{noise\ power\ at\ node\ z\ caused\ by\ R_S} \quad (1)$$

$$F_z = 1 + \frac{noise\ power\ at\ node\ z'caused\ by\ R_1,M_2,M_3,and\ R_2}{noise\ power\ at\ node\ z'caused\ by\ R_S} \quad (2)$$

$$F_z = 1 + \frac{R_0}{(g_{m1}X_0)^2R_S} + \frac{R_2}{4R_S} + \frac{R_4}{(g_{m1}g_{m4}X_0X_4)^2R_S} + \frac{\gamma}{(g_{m1}X_0)^2g_{m4}R_S\alpha_1^2\alpha_4^2} \quad (3)$$

$$F_{z\prime} = 1 + \frac{R_1}{R_S(g_{m2}X_1)^2\alpha_2^2} + \frac{\gamma}{g_{m2}R_S\alpha_2^2} \quad (4)$$

$$F = 1 + (F_Z - 1) + (F_{z\prime} - 1) \quad (5)$$

$$F = 1 + \frac{R_2}{4R_S} + \frac{R_0}{(g_{m1}X_0)^2R_S} + \frac{R_4}{(g_{m1}g_{m4}X_0X_4)^2R_S} + \frac{\gamma}{(g_{m1}X_0)^2g_{m4}R_S\alpha_1^2\alpha_4^2} + \frac{R_1}{R_S(g_{m2}X_1)^2\alpha_2^2} \quad (6)$$

Equations 7 and 8 give noise factors for $M1$ at z and z', and the term r is added as the relation of the two noise factors are presented in Equation 9. Furthermore, the term r indicates the fraction of noise of $M1$ at the output node.

In order to achieve complete noise cancellation, the term r must be equal to 1.

$$noise\ factor\ of\ M1\ at\ z = \frac{\left(\frac{4kT_\gamma}{g_{m1}}\right)\left(\frac{g_{m1}X_0}{1+g_{m1}(R_S||X_2)}\right)^2}{(g_{m1}(X_0||r_{01})^2 4kTR_S} \quad (7)$$

$$noise\ facor\ of\ M1\ at\ z' = \frac{\left(\frac{4kT_\gamma}{g_{m1}}\right)\left(\frac{X_2||R_S}{X_2||R_S + 1/g_{m1}}\right)}{4kTR_S} \quad (8)$$

$$r = \frac{Noise\ of\ M1\ at\ z}{Noise\ of\ M1\ at\ z'} \quad (9)$$

The schematic picture of the proposed LNA is depicted in Fig. 3. Moreover, additional gain stages including the feed-forward cascode CS stage, shown as A, boost the signal gain and the bandwidth of the amplifier. Furthermore, by combining the outputs of the gain stages using the associate adder circuit, we can achieve noise cancellation.

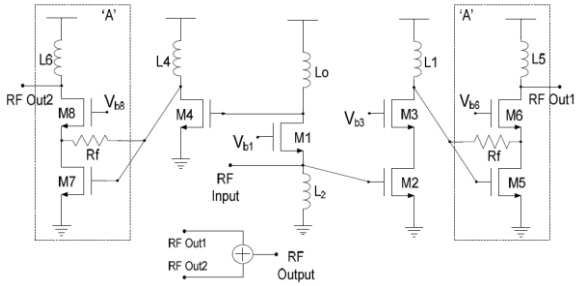

Fig. 3. The Proposed LNA with the Noise Cancellation Method.

Multi stage LNA proposes higher gain, in comparison with single stage LNAs. The noise performance of multi-stage LNA is not degraded, since the noise performance is mainly determined by the first stage. This can be shown using Frees noise equation:

$$F = F_1 + \frac{F_2 - 1}{G_1} + \cdots \frac{F_N - 1}{G_1G_2G_{n-1}} \quad (10)$$

$$g_{m2}RL = g_{m3}Rs \quad (11)$$

Where F is the total noise factor and Fi and Gi are the noise factor and power gain of i[th] stage. Normally the gain of first stage is high enough to suppress the effect of second stage in the total noise figure.

3. Results and analysis

The proposed LNA with noise cancellation can operate in frequencies ranging from 2.5 GHz to 4.5 GHz. The small size of the M1 transistor indicates the feature of matching the wideband input. The transconductance (g_{m1}) of M1 is set to 20 mS for 50Ω input matching with a bias current of 1.8 mA, while that of the L2 is 5.10 NH. This will help maintain the coefficient of the input reflection below -10 dB over the range of 2.5 GHz to 4.5 GHz. This is also depicted in Fig. 6. The transconductance (g_m) for M2 equals 43.53 mS; while it is equal to 43.56 mS for M3, and equal to 47.55 mS for M4. These are calculated based on the RF circuit design tradeoffs as well as the noise cancellation of M1 at the output node. Fig. 4 shows the

simulated noise value and the minimum noise value is equal to 3.17 dB. As can be seen in Fig. 5, there is an average power gain equal to 22.4 dB in the above-mentioned frequency range. On the other hand, Fig. 7 depicts a comparison of the simulated and the theoretical noise values, indicating a significant correlation between the figures. It is worth mentioning that the value of the simulated noise will increase as the frequency increases; this is due to the noise contribution from the circuit as well as parasitic parts that are neglected in the NF analysis; hence, they are not included in Equation 6. The proposed circuit provides flat stability, which is shown in Fig. 8. As can be seen in Fig. 9, there is linearity of -7.5 dB for the third-order intercept point (IIP3), which is acceptable. The LNA designed in this study uses thermal noise cancellation at the CG transistor of the first stage (i.e. M1), and Equation 6 is the basis for obtaining the curve for the theoretical noise value, which is then compared to the simulated noise value curve. It is concluded that in the frequency of 3 GHz, these two curves are closely similar. Tables I and II present the facet ratios and comparisons for the performance of various LNAs.

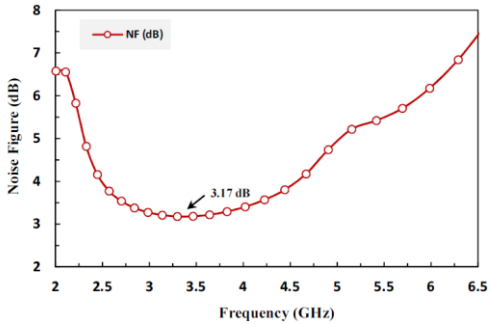

Fig. 4. The Curve Showing Simulated Noise Value for the LNA Proposed in the Study Equipped with Noise Cancellation.

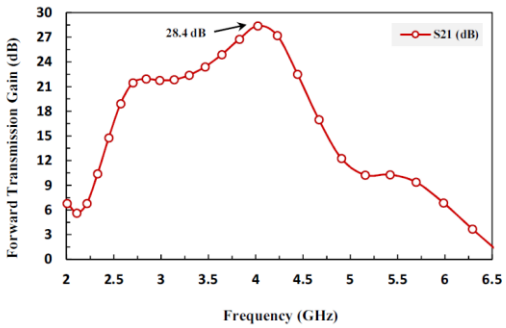

Fig. 5. The Curve Showing Simulated Power Gain for the LNA Proposed in the Study Equipped with Noise Cancellation.

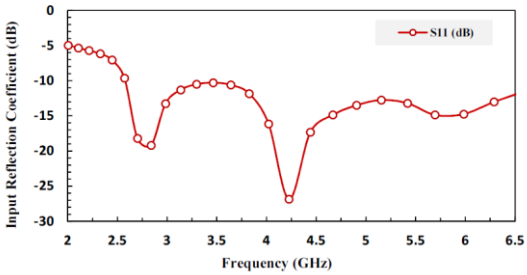

Fig. 6. The Curve Showing the Coefficient for Simulated Input Reflection for the LNA Proposed in the Study Equipped with Noise Cancellation.

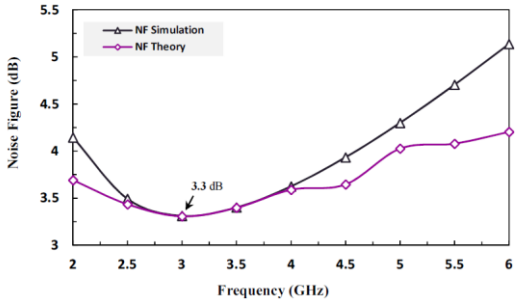

Fig. 7. Curves Showing Simulated and Theoretical Noise Values for the LNA Proposed in the Study Equipped with Noise Cancellation.

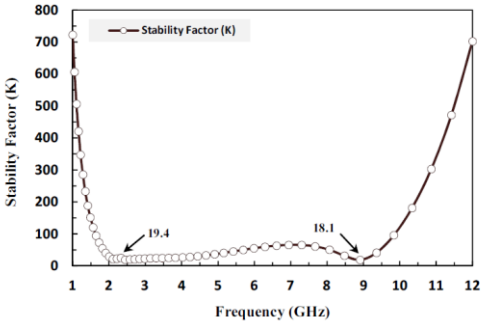

Fig. 8. The Curve Showing the Simulated Stability Factor for the LNA Proposed in the Study Equipped with Noise Cancellation.

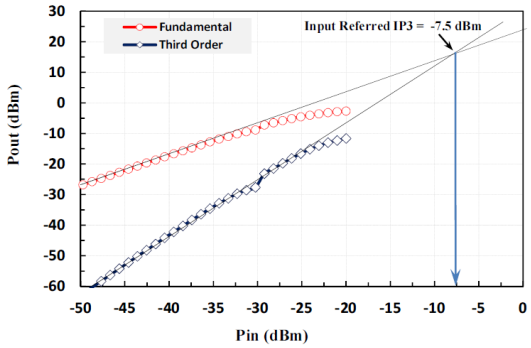

Fig. 9. The Curve Showing the Simulated IIP3 for the LNA Proposed in the Study Equipped with Noise Cancellation.

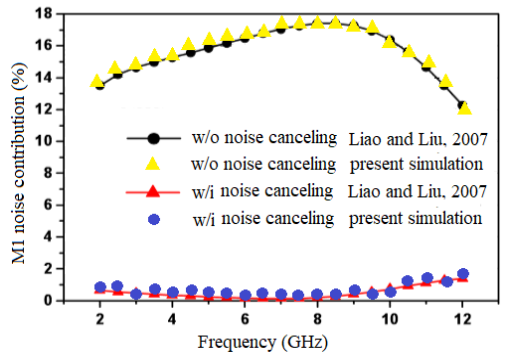

Fig. 10. Simulated noise contribution with and without noise canceling.

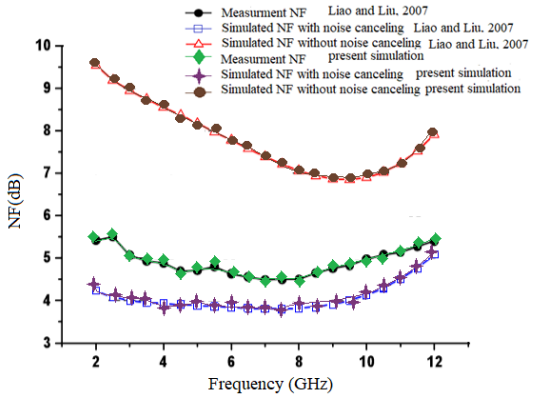

Fig. 11 Measured and simulated noise figures.

Table I. Aspect Rations and Parameter Values for the Presented Circuit.

Parameter	Value
$(W/L)_1$	$\mathbf{80\mu m/0.18\mu m}$
$(W/L)_{2,3,4,5,7}$	$\mathbf{120\mu m/0.18\mu m}$
$(W/L)_{6,8,n,p}$	$\mathbf{100\mu m/0.18\mu m}$
R_r	6K
L_o	9.13nH
L_1, L_4	3.88nH
L_2	5,88nH
V_{dd}	.8V
V_{b1}	00mV

Figs. 10 and 11 provide a comparison of the present modeling results with the results of previous researchers. As can be seen from the obvious figures, there is a good agreement between the results of the present modeling and the simulations of previous researchers.

In the frequency range of 2.5 to 4.5 GHz, a CMOS CG LNA has been used as the standard in the TSMC 0.18 μm CMOSRF technology. In this study, we analyze all the sources of noise in this configuration. Furthermore, a noise cancellation method is utilized in order to cancel the noise coming from the main sources of noise in the design. The results show a reduction of 22.49 percent in the noise using the proposed configuration compared to conventional LNAs that are not equipped with this type of noise cancellation. Moreover, over a spectrum of 2 GHz, a peak power gain of 28.4 dB and a base NF of 3.17 dB are achieved along with acceptable stability and linearity.

Table II. Performance of the LNA Proposed in the Study Equipped with Noise Cancellation for Technology ($\mu mCMOS$) and S11 (dB) < -10.

Parameter	Without Noise Cancellation [21]	With Noise Cancellation	
		Pre Layout	Post Layout
Frequency (GHz)	3.1~10.6	2.4~9.0	**2.4~4.5**
S21(ave) (dB)	17.70	24.24	22.40
S21(max) (dB)	21.60	28.49	28.40
NF (dB)	4.09	3.16	3.17
IIP3 (dBm)	-7.32	-7.34	-7.50

Moreover, a CMOS UWB LNA was designed using shunt-series inductive peaking and inter-stage matching. This design utilizes the source degeneration cascode configuration equipped with an inter-stage matching network. Furthermore, in this design, we placed a Chebyshev band pass filter at the input node while placing a shunt-series inductive peaking at the output node, resulting in better impedance matching and boosting the power gain.

3.1. Noise Analysis

The gain of the previous stage reduces the noise from the second stage in the proposed LNA. However, the primary stage determines the overall noise performance of the LNA [23]. The losses in the input matching network and the M1 transistor are the main causes of noise in the primary stage. Equation 12 provides the noise factor of the amplifier, $F(w)$. Moreover, the detailed derivations are provided in [5].

$$F(W) = 1 + \frac{P(W)\gamma}{G_m R_S a} \tag{12}$$

In which

$$p(W) = \frac{(pax)^2(1-|c|^2)}{1+2|c|pax+(pax)^2} + (wC_tR_S)^2(1+2|1+2|pax + (pax)^2) \tag{13}$$

In which, c is the coefficient of correlation between the gate noise and the drain noise; δ and γ are the surplus noise parameters, and α signifies the short channel effects. For CMOS devices, $\delta \approx 4, \gamma \approx 2, \alpha \approx 0.85, and\ c \approx 0.4\ j$ [24].

$$x = \frac{\delta}{5\gamma}; \rho = \frac{C_{gs}}{C_t}; \alpha = \frac{g_m}{g_{d0}} \tag{14}$$

According to Equation 12, while keeping all the other parameters constant, increasing the transconductance results in improved noise performance. The simulation results indicate that for a given current, there is a range for the value of M1 that leads to the simplest noise value over the bandwidth. Fig. 12 depicts a noise model for the input matching network.

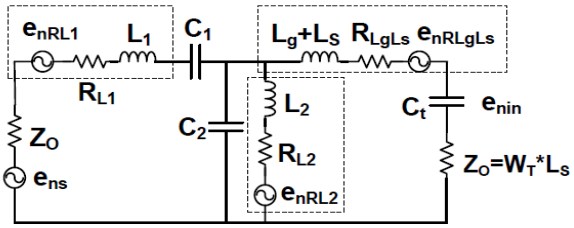

Fig. 12. The Noise Model for the Input Matching Network.

The elements of the Chebyshev filter include L_1 and C_1. R_{L1} is the parasitic resistor of L_1, while R_{L2} and $R_{L_gL_S}$ are the parasitic resistors of L_2 and $L_g + L_S$, respectively. The voltage sources e_{nRL_1}, e_{nRL_2}, and e_{nRL_S} signify the thermal noises created by resistors R_{L1}, R_{L2}, and R_{LgLs}, respectively. Equations 15, 16, and 17 present the transfer functions for these sources of noise.

$$TF_{RL1} = \frac{e_{nin}}{e_{nRL1}} = \frac{w(s)}{[W(s)+1]sC_tR_S} \quad (15)$$

$$TF_{RL2} = \frac{e_{nin}}{e_{nRL2}} = \frac{\left(\frac{1}{sC_2}\right)||Z_{gs}||Z_1}{Z_2+\left(\frac{1}{sC_2}\right)\|Z_{gs}\|Z_1} \times \frac{1}{Z_{gs}(sC_t)} \quad (16)$$

$$TF_{RL2} = \frac{e_{nin}}{e_nR_{LgLs}} = \frac{1}{Z_{gs}+(\frac{1}{sC_2})\|Z_1\|Z_2} \times \frac{1}{(sC_t)} \quad (17)$$

In which

$$Z_2 = SL_2 + R_{L2};$$

$$Z_{gs} = s(L_g + L_s)R_{LgLs} + \frac{1}{(sC_t)} + Z_0;$$

$$Z_1 = sL_1 + RL_1 + \frac{1}{(sC_1)} + Z_0$$

In which, $W(s)$ is the performance of the filter transfer, and for the second-order Chebyshev filter, $Z_1 = Z_0$. The noise generated by the passive devices of the third-order filter is much larger than the noise created by the second-order filter. Therefore, using a second-order Chebyshev filter is much better for reducing noise.

3.2. Results of the Simulation

In this section, the simulation results for UWB LNA are presented. The noise value depicted in Figure 11 indicates a great performance equal to 3.42 dB to 6.85 dB in the frequency range of 3.1 GHz to 10.6 GHz. The power gain ranges from 11.11 dB to 17.12 dB over the selected bandwidth. This finding indicates a gain roll-off at higher frequencies; this can be due to the shunt-series inductive peaking. The input reflection coefficient is presented in Figure 13. In this figure, the constant S11 over the range of frequencies from 3.1 to 10.6 GHz indicates the satisfactory design of the input matching network. The performance of the LNA is summarized in Table 3. Figure 14 depicts the general layout of the proposed LNA on a 0.9 mm×1 mm space. The simulations are carried out using the TSMC 0.18 µm CMOS technology.

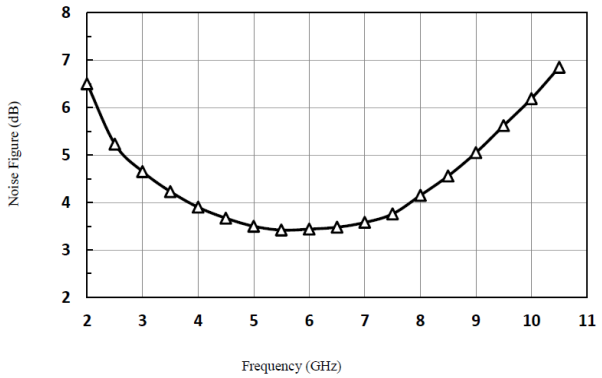

Fig. 13. Simulated Noise Values for the Proposed LNA.

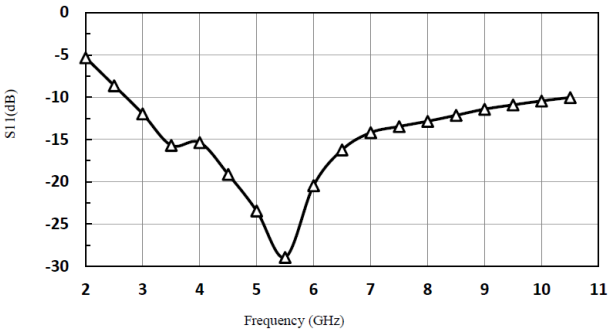

Fig. 14. Simulated Coefficients for Input Reflection.

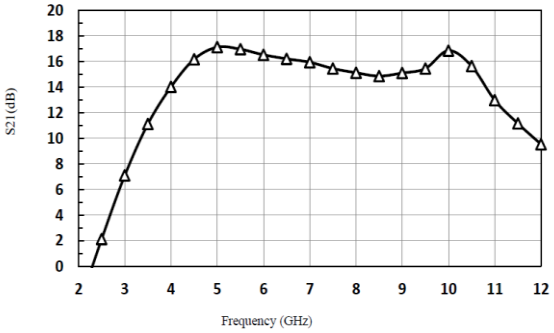

Fig. 15. Simulated Gains for Forward Transmission.

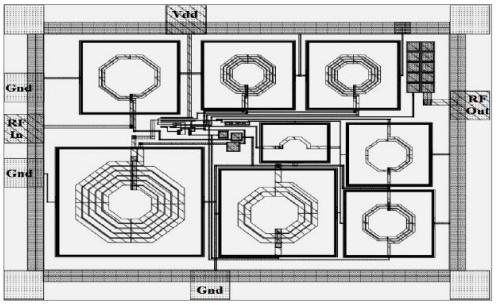

Fig. 16. General Layout of the Proposed LNA.

Table 3. Performance of the Proposed UWB LNA.

Parameters	Freq (GHz)	Gain (dB)	NF (dB)	S11 (dB)	Power (mW)
Values	3.1-10.6	11.11-17.12	3.4-6.7	< -10	11.2

4. Conclusions

The current study proposes a method of noise cancellation for the CMOS low-noise amplifier, which reduces the noise and boosts the gain. This is a completely novel method as far as we know. In order to cancel the dominant noise, we analyze the noise contributions from different passive and active components of the three-stage CG LNA. The input matching device, which is the first CG transistor, is the main source of the noise. In this design, we made use of the Chebyshev band pass filter in order for the input matching and inter-stage matching network to hold forward the needed signal through bypassing the unnecessary signal. On the other hand, in order to compensate for the gain roll-off at higher frequencies, a shunt-series inductive peaking network is utilized in the design.

The results of the study show that thermal noise from the matching devise is the main source of noise in the system. The second-stage common-source transistor's noise contribution is very close to corner frequencies. This is due to the narrow-band characteristics of the common source amplifier. In contrast, the common gate amplifier shows wide-band characteristics and its noise contribution remains approximately constant (2.8±0.3) over the frequency range. In this study, a novel noise cancelling LNA is designed in order to mitigate the noise generated by the matching device. The results show that the proposed configuration provides a 22.49 percent reduction in the noise value compared to a conventional LNA not equipped with noise cancellation. Moreover, equations for the overall noise factor and conditions for cancelling noise are obtained. Finally, the proposed LNA provides a peak power gain of 28.4 dB as well as a base NF equal to 3.17 dB over the 2 GHz spectrum, with acceptable stability and linearity.

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