An Active, Low-Power, 10Gbps, Current-based Transimpedance Amplifier in a Broadband Optical Receiver Front-End

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Abstract

An integrated CMOS, low-power optical communication receiver front-end is designed and presented in this paper for specified applications of 10Gbp/s. The transimpedance amplifier (TIA) stage and the limiting amplifier (LA) stage possess an active feedforward network based on current-mirror topologies and differential topologies, respectively. In order to obtain broadband performance, low-power consumption characteristic and low-occupied area on chip, an active type of inductors are employed in the TIA as well as the LA stage. The performance of the optical system is simulated using 90 Nano-meter CMOS technology parameters, which exhibits power dissipation of only 1.5mW, -3dB frequency of 6.92GHz, 24pA/√Hz input referred noise, and transimpedance gain of 40.1dB ohm for the TIA stage, while, the whole optical receiver front-end consumes 7.7m Watt, providing 71.4dB ohm gain beside acquiring 6.55GHz frequency bandwidth. Finally, the performance of the presented optical receiver front-end as a low-power, 10Gbps block-diagram is justified.

Keywords

Low-Power, Transimpedance Amplifier, Limiting Amplifier, Optical Receiver, 10Gbps.

1. Introduction

In an optical receiver system for communication applications, the circuitry of Transimpedance Amplifier (known as TIA) plays a very especial role as the 1st stage of a receiver system [1]. The TIA building block, which determines the basic specifications of an optical communication receiver such as wide bandwidth frequency, high conversion gain and low noise, is placed after the photodiode as the first stage of the optical front-end. The TIA circuitry is responsible to convert the produced current of the photodiode (PD) into an amplified voltage [2], while, in CMOS TIAs the signal bandwidth has to be severely compromised with the noise performance and transimpedance gain, especially when the TIA is to operate at high data rates.

At the input node of the TIAs, large time constant is usually formed due to the high value of parasitic capacitance of the PD, which creates a low-frequency pole and decreases the circuit frequency bandwidth. That is why the input resistance of TIA stages need to be properly designed to be low. Moreover, in order to reduce the number of amplifying stages at the analogue circuitry of the receivers, the gain of the TIA circuitry must be as high as possible. In addition, as the TIA stage is situated at the first stage of receivers, it is necessary to keep the noise of the TIA stage as low as possible. So, a high gain TIA stage reduces the effect of the noise by increasing the value of SNR [3]. However, when the resistance of the TIA circuitry at output node is high, the low frequency pole formed at the output lessons the -3dB frequency of the circuit. The out put resistance of the TIA stage is of interest when a proceeding stage, which is mainly a limiting amplifier (LA) or an automatic gain controller (AGC), with high input resistance and parasitic capacitance is connected to the TIA circuit, as it is demonstrated in figure (1). Different topologies have been reported till now to isolate the large parasitic input capacitance of the photo-diode and to achieve the above mentioned specifications (low-input resistance, low-output resistance, low power and high transimpedance gain) such as: Shunt resistance [4], common gate (CG) topology [5], regulated cascode circuit (RGC) [6-8], common source employing shunt feedback [9], cross-coupled current conveyor [10] and inverter-based topologies [11]. CG topologies are not capable of providing proper transimpedance gain and RGC structures are not capable of operating well at low supply voltages. In comparison with other structures mentioned above, the cross-coupled current conveyor structure, which creates a zero differential impedance at its input, is capable to isolate the large capacitance of the photodiode more effectively.

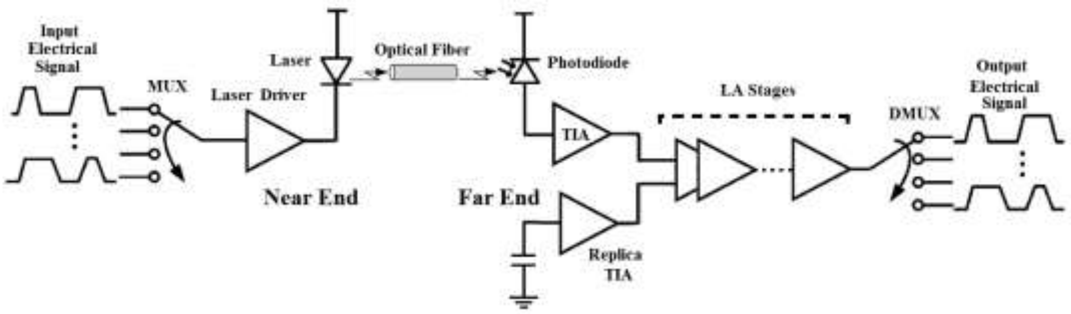


Fig. 1. Demonstration of a transimpedance amplifier in a system of optical receiver

Moreover, Active voltage-current Feedback [12] Shunt inductive peaking technique, series inductive peaking technique [13] and the combination of these techniques [14–15] are also reported to increase the data rates of TIA circuits by creating resonant peaking in the frequency response of the TIAs, in which using passive inductors yields high occupied area on chip. Also, series inductive peaking technique has been reported in [16], where it is used in amplifiers in order to absorb few parasitic capacitances into some transmission lines along the output and input transmission lines; and also has been reported in [17], where it is used at input node of an inverter structure in order to extend further the frequency bandwidth, in cost of higher occupied chip area. Also, Fully Differential Structures can be a good candidate as low-noise amplifiers [18].

In this paper, in addition to handle the above mentioned specifications, it has been tried to reduce the power dissipation of the circuit by reducing the output & the input resistance of the presented TIA, and providing a zero using active elements at output node to create a peaking in the frequency response, which benefits from not occupying large area on chip in comparison with conventional peaking techniques. A diode-connected transistor is also used at the input of the TIA, which yields low input resistance, while the feedforward network is designed with active elements to ease the process of fabrication. The transimpedance gain is also obtained based on current mirror topologies.

So, here is the organization of this paper. Section 2 presents the proposed TIA and the related mathematical terms and discussions. Section 3 deals with the LA stages in a similar way. Simulation results of the presented TIA and the LA stages are given in section 4, while the performance of the whole receiver front-end is analyzed in section 5 and finally, conclusions are given in section 6.

2. The Proposed TIA

Figure (2) and figure (3) demonstrate the proposed active, current-mirror based TIA circuit, and the open-loop AC equivalent circuit model of it, respectively.

This circuit is based on current-mirror topologies. The signal is amplified through two different paths, which are finally summed at output node. In the first path, the signal passes through M_1-M_2-M_4-M_5, which is amplified proportional to widths of these transistors as $\frac{W_2}{W_1} \times \frac{W_5}{W_4}$. In the second path, the signal passes through M_1-M_3, which is amplified proportional to widths of these two transistors as $\frac{W_3}{W_1}$. These two paths finally meet each other at output node and the amplified signals are summed there.

The AC equivalent circuit demonstrates the most effective equivalent elements. The main signal from the photodiode (I_{in}) experiences the summation of the parasitic photodiode capacitance (C_{pd}) and parasitic gate-source capacitances of M1, M2 and M3 (which affects the -3dB bandwidth) in the input node, in parallel with the small input resistance of $(g_m)^{-1}$ (M1 as diode connected). M2 produces a current according to V_{gs1} (g_{m2}*V_{gs1}), which is then multiplied by $(g_{m4})^{-1}$ (It is worth noting that r_{o2} in parallel with $(g_{m4})^{-1}$ is approximately equal to $(g_{m4})^{-1}$, so r_{o4} can be neglected). Finally, in the output node two current sources are producing currents according to V_{gs1} and V_{gs4}, with a load (M_6 and M_7), in which the load is equal to $(g_{m6})^{-1}$ at low frequencies, and at high frequencies it behaves like an inductor, as it shown in the following.

Hence, the open-loop transresistance gain of the proposed current-based transimpedance amplifier can be written according to equation (1), for low frequencies.

$$A_Z = \frac{V_{out}}{I_{in}} = \left(\frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} \times \frac{\left(\frac{W}{L}\right)_5}{\left(\frac{W}{L}\right)_4} + \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} \right) \times \frac{1}{\frac{r_{o3}+r_{o5}}{r_{o3}\times r_{o5}} + g_{m6}} \quad (1)$$

In which W and L are the width and length of a MOS transistor, respectively, r_o is the drain-source resistance and g_m is the transconductance of a MOS transistor.

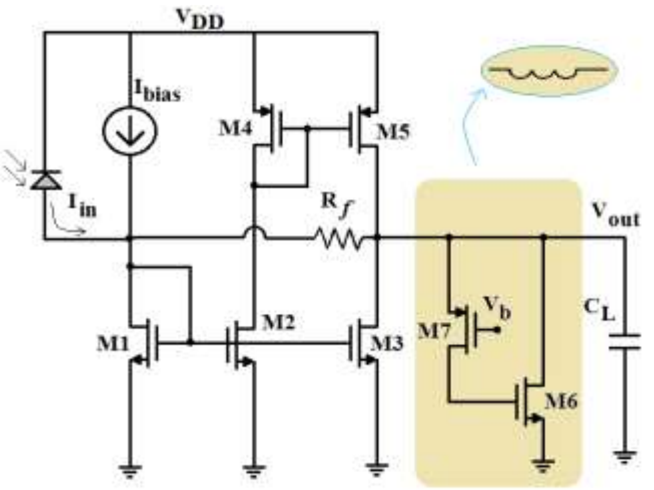


Fig. 2. The Proposed current-mirror based TIA Circuit

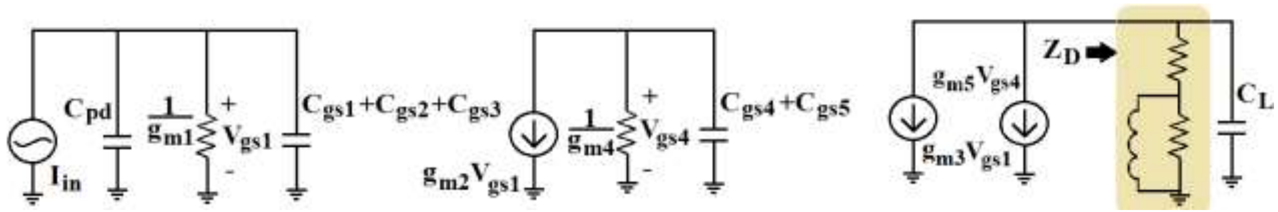


Fig. 3. Equivalent Circuit of the open-loop current-based Transimpedance amplifier

Due to the use of a diode-connected structure, a low value of $(g_{m1})^{-1}$ can be considered as its resistance at the input node. As it is required to obtain a wide -3dB frequency bandwidth, it is essential to reduce the input resistance by changing the width of W_1. Using a proper feedback (R_f), as in figure (2), also helps to reduce the output and input resistances in cost of less transimpedance gain. Hence, the time constants at these nodes experience a reduction and these two poles move further from the origin. Consequently, an extended -3dB frequency bandwidth is obtained.

So, for the presented current-based TIA, the input resistance can be defined as equation (2).

$$R_{in} = \frac{R_f}{(g_{m1} \times R_f + 1) \times \left(1 + \frac{A_Z}{R_f}\right)} \tag{2}$$

And equation (3) provides total capacitance at the input node, which is approximately equal to the capacitance of the photodiode, due to its relatively large value.

$$C_{in} = C_{pd} + C_{gs2} + C_{gs1} \approx C_{pd} \tag{3}$$

Here, C_{gs} defines the gate-source capacitance of a MOS transistor and C_{pd} defines the parasitic photodiode capacitance.

As it was discussed before, the capacitance of the photodiode (C_{pd}) is relatively large, so equation (3) is approximately equal to C_{pd}. Hence, the input pole of the circuit is defined as equation (4).

$$S_{Pin} = -\frac{(g_{m1} \times R_f + 1) \times \left(1 + \frac{A_Z}{R_f}\right)}{C_{in} \times R_f} \tag{4}$$

An active type of inductor at the output is created by employing combination of M_6 and M_7. This active inductor starts to resonate with the load capacitance, and this phenomenon introduces a zero inside the transfer function of the current-base TIA, which cancels the effect of output pole and consequently the performance of the circuit will speed up and so the -3dB frequency is extended. M_6 behaves as an inductor, while M_7 operates in triode region. Existence of a zero in the transfer function makes it possible to reduce the passing DC current, while a proper frequency response can be achieved. So, not only the -3dB bandwidth is now extended, but also the power dissipation is reduced. It must be noted that this reduction in the power dissipation is obtained in cost of higher thermal noise. Of course, the thermal noise can be controlled to some extend using the negative feedback network [3]. The feedback network affects on thermal noise, which is analyzed in the following sections.

Furthermore, figure (4) demonstrates the equivalent circuit model of M_7-M_6, in which by writing terms of a KVL and a KCL as follows, we have:

$$V_{gs6} \times C_{gs6} \times s + g_{m6} \times V_{gs6} = -I_x \tag{5}$$

$$V_{gs6} \times C_{gs6} \times r_{o7} \times s + V_{gs6} = -V_x \tag{6}$$

Here, V_{gs} refers to the gate-source voltage of a MOS transistor. Moreover, having equations (5) and (6) and neglecting the channel-length modulation for simplicity, the impedance of the combination of M_6-M_7 at the output could be expressed as equation (7) [3].

$$Z_D = \frac{V_x}{I_x} = \frac{r_{o7} \times C_{gs6} \times S + 1}{g_{m6} + C_{gs6} \times S} \tag{7}$$

Where the value of the active inductor is expressed as equation (8).

$$L = \frac{C_{gs6}}{g_{m6}}\left(r_{o7} - \frac{1}{g_{m6}}\right) \tag{8}$$

The total impedance of the output node is the result of three parallel impedances, thus the output impedance is quite low and again the feedback network makes it even less. By neglecting the channel-length modulation of M_3 and M_5 for simplicity, the low frequency output impedance is expressed as follows:

$$Z_{out} = \frac{R_f}{[R_f \times g_{m6}+1] \times \left[1+\frac{A_Z}{R_f}\right]} \tag{9}$$

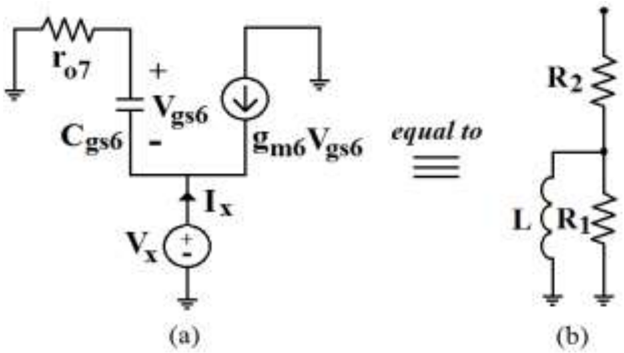


Fig. 4. Active inductor implementation using M_6 and M_7 (a) Small signal circuit model of M_6, M_7 (b) Equivalent active inductor model consists of M_6, M_7

And the open-loop, high-frequency, output impedance could be expressed as follows:

$$Z_{out} = r_{on}\|r_{op}\|Z_D = \frac{(r_{07}\times C_{gs6}\times S+1)r_{0n}\times r_{0p}}{[(1+S\times r_{o7}\times C_{gs6})(r_{op}+r_{on})+(S\times C_{gs6}+g_{m6})(r_{op}\times r_{on})]} \tag{10}$$

Hence, the output pole shall be given as equation (11).

$$S_{Pout} = -\frac{1}{C_{out}\times R_{out}} \tag{11}$$

Where, R_{out} is the output resistance and C_{out} can approximately be written as follows:

$$C_{out} = C_L + C_{db5} + C_{dg5} + C_{db3} + C_{dg3} + C_{dg6} + C_{db6} + C_{sg7} + C_{sb7} \tag{12}$$

As it is mentioned before, using feedback network reduces the rate of the noise, extends the -3dB frequency and decreases the rate of the gain. The transimpedance gain with two poles and one zero is approximately equal to equation (13), in which the zero is embedded in the Z_{out}. By assuming equal channel-length for each transistor, and also assuming $A_{Zf} = \frac{V_{out}}{I_{in}}$ as the closed-loop gain of the proposed current-based transimpedance amplifier at low frequencies, the transfer function of the proposed amplifier is expressed as equation (13).

$$A_{Z(s)} = \frac{A_{vf}\times(r_{07}.C_{gs6}.S+1)}{\left(S+\frac{(g_{m1}.R_f+1)\times\left(1+\frac{A_{Zf}}{R_f}\right)}{C_{in}\times R_f}\right)\times\left(S+\frac{1}{C_{out}\times R_{out}}\right)} \tag{13}$$

Where,

$$A_{Zf} = \frac{V_{out}}{I_{in}} = \frac{1}{\frac{\left(\frac{r_{o3}+r_{o5}}{r_{o3}.r_{o5}}\right)+g_{m6}}{\left(\frac{W_2.W_5}{W_1.W_4}+\frac{W_3}{W_1}\right)}+\frac{1}{R_f}} \tag{14}$$

At the node in drain of M2, r_{O2} is in parallel with $(g_{m4})^{-1}$ which is approximately equal to $(g_{m4})^{-1}$, so r_{O4} can be neglected. At the output node (equations (1) and (14)) r_{O3} and r_{O5} are in parallel with $(g_{m6})^{-1}$, which can be neglected at low frequencies $\left(\frac{r_{o3}+r_{o5}}{r_{o3}.r_{o5}} + g_{m6} \approx g_{m6}\right)$. But at high frequencies M7, as a resistor (ro7), forms a zero with M6 in the transfer function. So, in equations (7) and (8), r_{O7} is mentioned and their effect is shown as an equivalent inductor in figure (3).

As the above mentioned zero resonates with the pole of output load, equation (13) can be approximated as a single-pole function as in equation (15).

$$A_{Z(s)} \approx \frac{A_{Zf}}{S+\frac{(g_{m1}.R_f+1)\times\left(1+\frac{A_{Zf}}{R_f}\right)}{C_{in}\times R_f}} \tag{15}$$

Hence, as the input pole is known to be dominant pole according to equation (15), the -3db frequency can approximately be calculated as in equation (16).

$$f_{-3db} \approx \frac{(g_{m1}.R_f+1)}{2\pi.C_{pd}.\ R_f}\left(1+\frac{A_{Zf}}{R_f}\right) \tag{16}$$

As it can be concluded from equation (16), in order to enlarge the -3dB frequency of the circuit, $\frac{A_{Zf}}{R_f}$ needs to be increased.

Moreover, although the noise of TIA stage can be considerably decreased in differential LA stages as the common mode, it is necessary to analyse the performance of noise in the presented transimpedance amplifier due to the fact that high-gain, low-noise TIA structures can guarantee the proper performance of whole optical receiver front-end.

Figure (5), demonstrates the equivalent noise circuit of the presented circuit, in which each noise source is shown as a current source.

By considering equation (17), the input referred noise current of I_{n3} and I_{n5} due to the thermal noise of M_3 and M_5 are given by equations (18) and (19), respectively.

$$I_{D3} = \frac{\left(\frac{W}{L}\right)_3}{\left(\frac{W}{L}\right)_1} I_{D1} \tag{17}$$

$$\overline{I^2_{noise,in\ M3}} = 4KT\gamma g_{m3} \times \left(\frac{g_{m1}}{g_{m3}}\right)^2 = 4KT\gamma g_{m3} \times \left(\frac{\sqrt{2\mu_n.C_{ox}\left(\frac{W}{L}\right)_1.I_{D1}}}{\sqrt{2\mu_n.C_{ox}\left(\frac{W}{L}\right)_3.I_{D3}}}\right)^2 = 4KT\gamma g_{m3} \times \left(\frac{1}{\frac{W_3}{W_1}}\right)^2 \tag{18}$$

$$\overline{I^2_{noise,in\,M5}} = 4KT\gamma g_{m5} \times \left|\frac{g_{m4}}{g_{m5}} \times \frac{g_{m1}}{g_{m2}}\right|^2 = 4KT\gamma \frac{1}{g_{m5}} \times \left|g_{m4} \times \frac{g_{m1}}{g_{m2}}\right|^2 \quad (19)$$

In which γ refers to the noise factor of a MOS transistor.

Also, by considering equation (20), the input referred thermal noise produced by M_2 and M_4 can be expressed using equations (21) and (22), respectively.

$$I_{D2} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_{D1} \quad (20)$$

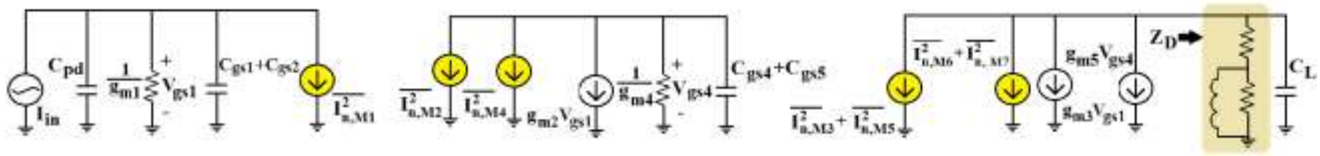


Fig. 5. Equivalent Thermal Noise Circuit of the TIA

$$\overline{I^2_{noise,in\,M2}} = 4KT\gamma g_{m2} \times \left|\frac{g_{m1}}{g_{m2}}\right|^2 = 4KT\gamma g_{m2} \times \left(\frac{\sqrt{2\mu_n.C_{ox}\left(\frac{W}{L}\right)_1.I_{D1}}}{\sqrt{2\mu_n.C_{ox}\left(\frac{W}{L}\right)_2.I_{D2}}}\right)^2 = 4KT\gamma g_{m2} \times \left(\frac{1}{\frac{W_2}{W_1}}\right)^2 \quad (21)$$

$$\overline{I^2_{noise,in\,M4}} = 4KT\gamma g_{m4} \times \left|\frac{g_{m1}}{g_{m2}}\right|^2 \quad (22)$$

M_1, whose thermal noise is equal to $4KT\gamma g_{m1}$, adds directly its thermal noise to the input node. But as it is located in parallel with the parasitic input capacitance, the thermal noise generated by M_1 is negligible, and the thermal noise of C_{pd} can be written as equation (23) [19, 20].

$$\overline{I^2_{noise,in\,M1}} = \frac{KT}{C_{pd}} \quad (23)$$

As it can be concluded from equations (18) and (21), by decreasing the width of W_1, not only the referred thermal noises of M_3 and M_2 at the input are decreased, but also more transimpedance gain can be obtained. Moreover, thermal noise of M_7 and M_6 are also divided by $(A_Z)^2$, which is a high value.

3. LA Structure

The block diagram and the structure used for the LA cell gains are presented in figure (6). As an extended width is required for high bit rates and the width of a transistor is not supposed to be too large, the drain-source terminals of two transistors (M_{19} and M_{37}) are connected in parallel, so that the AC signal could be amplified by two times of g_m (g_{m19}+ g_{m37}) and therefore, extra gain can be achievable from each cell. Of course, this extra gain is obtained in cost of more thermal noise. Moreover, M_{21} and M_{23} provide an active inductor load, which forms a zero inside the transfer function of each LA cell gain. Having a zero in transfer function yields an extended frequency bandwidth. Hence, a proper frequency response can be achieved consuming less power.

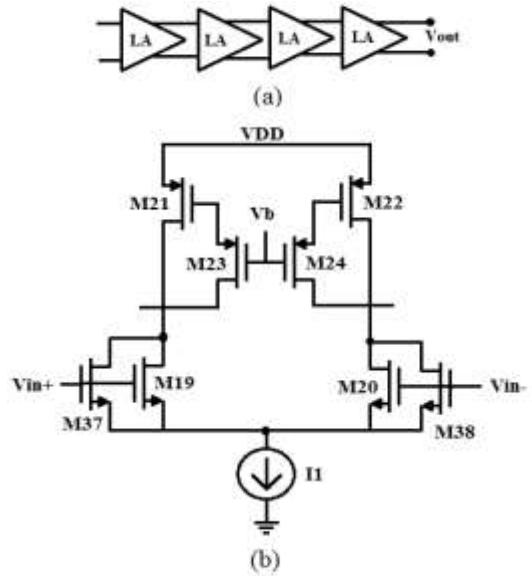


Fig. 6. (a) Block Diagram of the LA stage. (b) Structure of Each Cell Gain.

The equivalent circuit of each cell gain is demonstrated in figure (7), using half circuit model. So, by assuming drain source of M_{19} and M_{37} equal to r_{ON}, output impedance of each cell gain can be written as equation (24), while, the total capacitance at the output can be calculated as equation (25).

$$Z_{out,LA} = \left(\frac{1}{r_{oN}} + \frac{1}{r_{oN}} + \frac{1}{Z_D}\right)^{-1} = \frac{r_{oN}.(1+r_{o23}.\ C_{gs21}.S)}{2(1+r_{o23}.\ C_{gs21}\ .S)+ r_{oN}\ (g_{m21}+C_{gs21}.S)} \quad (24)$$

$$C_{out,LA} = \left(C_{gd19} + C_{gd27}\right)\left(1 - {}^{1}/_{A_v}\right) + C_{gd23} + C_{gd21} + C_L \quad (25)$$

In which A_V defines the gain of each cell. So, the created pole at the output is equal to $S_P = \frac{1}{R_{out}.C_{out}}$. The zero, which is created by M_{21} and M_{23}, starts to resonate with $C_{out.}$.

In this design, the post amplifier consists of four stages of LA cell. By assuming that each cell gain of the LA structure introduces two poles, the transfer function of each cell gain is defined as equation (26).

$$A(s) = \frac{A_v. w_n^2}{s^2+2\xi w_n.s+ w_n^2} \quad (26)$$

In which A_v is the small signal gain, and ξ is the corresponding damping factor. So, the -3db frequency for each cell gain can be written as equation (27) [21].

$$w_s = \left[1-2\xi^2+\sqrt{(1-2\xi^2)^2+1}\right]^{1/2}.w_n \quad (27)$$

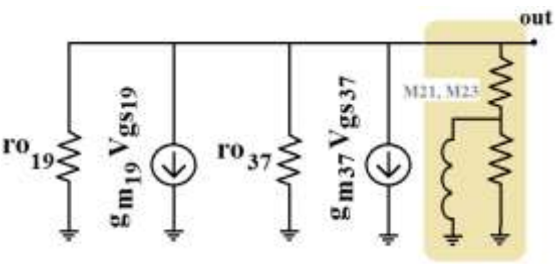


Fig. 7. Equivalent half circuit model of each LA cell

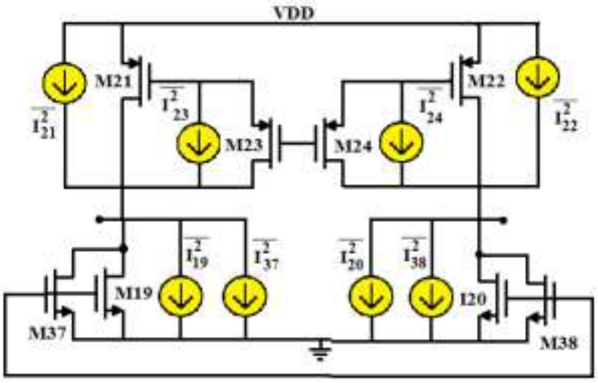


Fig. 8. Demonstration of noise sources in each LA cell

Then, for four stages of cascaded LAs, the -3db frequency is as follows [21]:

$$w_C = \left[1-2\xi^2+\sqrt{(1-2\xi^2)^2-1+2^{\frac{1}{4}}}\right]^{1/2} \times w_n \quad (28)$$

ξ is supposed to be √2/2 whenever a flat response is expected. Of course, these equations are true as long as amplifiers operate at small signal.

So, according to equations (27) and (28), cascading stages result in a decreased frequency bandwidth. So, each call gain must provide more than enough bandwidth (w_s), so that proper frequency bandwidth can be obtained after cascading four stages.

Moreover, figure (8) demonstrates noise sources in LA stages, in which the produced noise sources are shown as current sources. As it is discussed before, M_{19} and M_{37} provide extra gain in cost of more thermal noise.

Representing the uncorrelated thermal noise of each transistor using current sources, output thermal noise can be defined using half circuit model, as in equation (29).

$$\overline{V_{out}^2} = 4KT\gamma(g_{m19}+g_{m37}+g_{m21}+g_{m23})\times(Z_{out,LA}\|r_{o19}\|r_{o37})^2 \quad (29)$$

4. Simulations and Analysis

The performance of the presented TIA circuit is verified through the following analysis using 90nm CMOS technology parameters. Figure (9) demonstrates the frequency response of the current-based transimpedance amplifier, showing 40.1dBΩ transimpedance gain beside about 0.35dB peaking, which proves the proper performance of M6 and M7 in the circuit, as an active inductor. This active inductor forms a zero, which starts to pull up the frequency response at 300MHz. The effect of this zero is cancelled by a pole, and the frequency response starts to fall down at 2.5GHz. Finally, the -3dB frequency of the circuits is equal to 6.92GHz. Moreover, by using 1 volt supply, the dissipating power is equal to 1.5 milli-Watt.

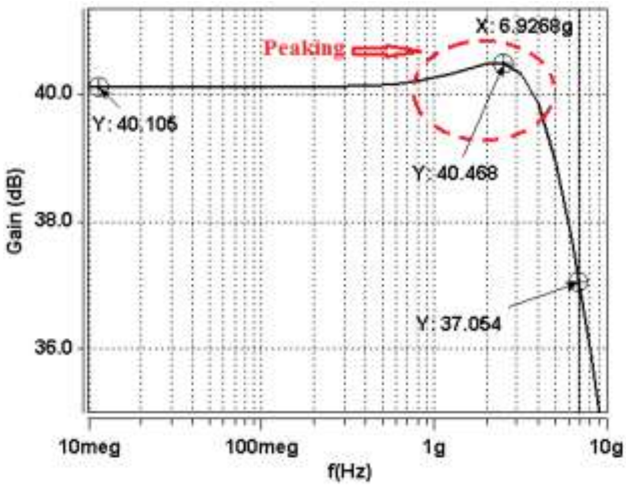


Fig. 9. Frequency Response

Moreover, analyzing the output signal of the transimpedance stage is always of interest especially for communication applications. So, the eye diagram of the current-based circuit amplifier is demonstrated in figure (10) using PRBS 2^7-1with 200μ Ampere input signal. As in figure (10), the eye is clearly opened about 25mV.

Reducing the input resistance of any TIA stage is essential to achieve broadband characteristics, as discussed before. In figure (11-a) the input impedance/resistance of the TIA structure is demonstrated over frequency, while, in figure (11-b) the input resistance of the closed-loop and the open-loop TIA is compared. As it can obviously be concluded from figure (11-b), the feedback network has a great influence in reducing the input resistance, due to the fact that the input resistance at low frequencies decreases from 1044.8Ω to 55.9Ω, which shows 18.6 times reduction.

Additionally, as fabrication errors in ICs may cause unwanted changes due to variations of the transistor dimensions (Widths and Lengths with 0.03 deviation), Monte-Carlo simulations over frequency response for investigating the performance correctness of the proposed circuit is done. Within the Monte-Carlo analysis, the effect of non-idealities over the fabrication process is analyzed. The number of runs is considered to be 100 in this analyze. Results over the frequency response and the value of gain are demonstrated in figure

(12-a) and figure (12-b), respectively, which show the mean value of 40.16dBΩ and standard deviation of 0.22dBΩ for the gain value.

Furthermore, the frequency response of the transimpedance circuit is analyzed over different temperatures. For 120ºC variations, the gain value varies for 1.4dB, while, the bandwidth varies for 0.85GHz. Also, the active inductor forms a greater peaking at low temperatures, as in -30ºC, the peaking rises up to 1.8dB (figure 13). As in table (1), which summarizes the effect of temperature over these three parameters, it can be concluded that by increasing the temperature, the transimpedance gain increases, while the frequency bandwidth decreases, due to the fact that the peaking also fades away.

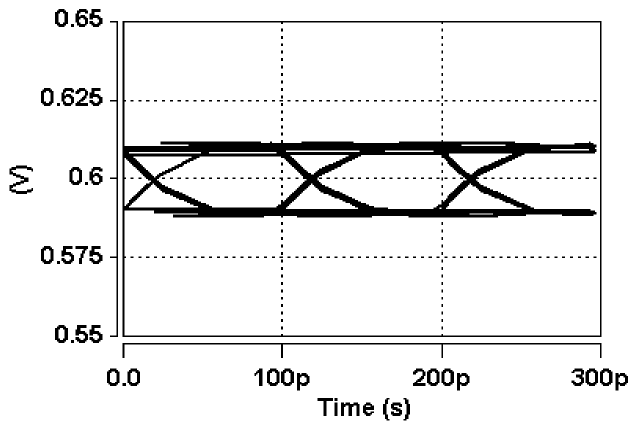
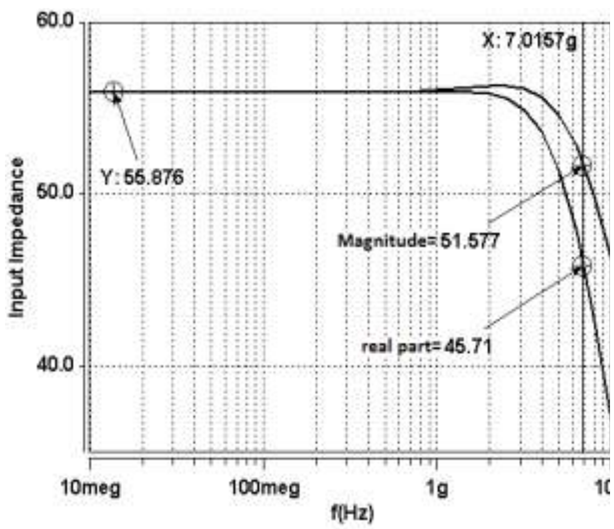
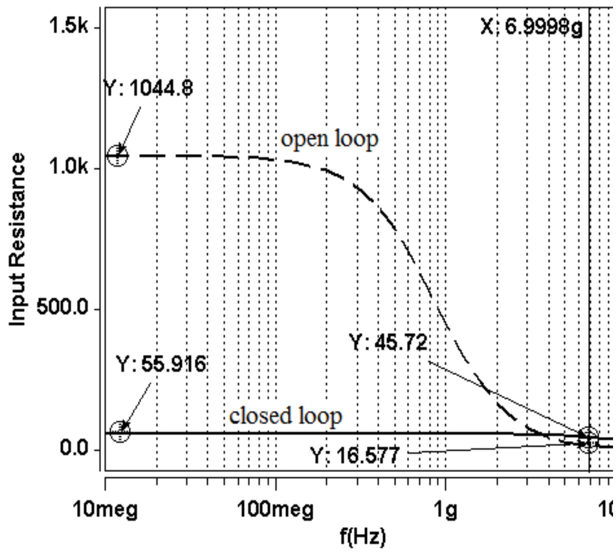


Fig. 10. Eye diagram



(a)



(b)

Fig. 11. (a) Input Impedance and input resistance, (b) effect of feedback network on the input resistance

In addition, effect of supply voltage variation on characteristics of the presented TIA is also analyzed and the results are briefly given in table (2). Increasing the supply voltage results in bandwidth reduction, while the power consumption increases and the peaking in frequency response fades away.

Moreover, as it was expected the input resistance of the open-loop current-based circuit is considerably depended on the transconductance of M1 (g_{m1}). Table (3) and figure (14) provide an analysis over the width of M_1, which is diode-connected, and the open-loop input resistance, respectively. By increasing the width of M_1, input resistance decreases considerably as $R_{in}=(g_{m1})^{-1}$, as expected.

Furthermore, the noise performance of the presented transimpedance amplifier at output node is demonstrated in figure (15). The low frequency output noise is equal to 3.3nV/√Hz, which reduces to 1.4nV/√Hz@-3dB frequency. Also, the feedback network is omitted in the presented circuit to analyze the noise performance and the momentous of the feedback network on the noise value. Figure (16) compares the open-loop and the closed-loop noise performance curves of the transimpedance amplifier. Table (4) compares these two curves, overly. It is shown that the feedback network significantly lessons the noise.

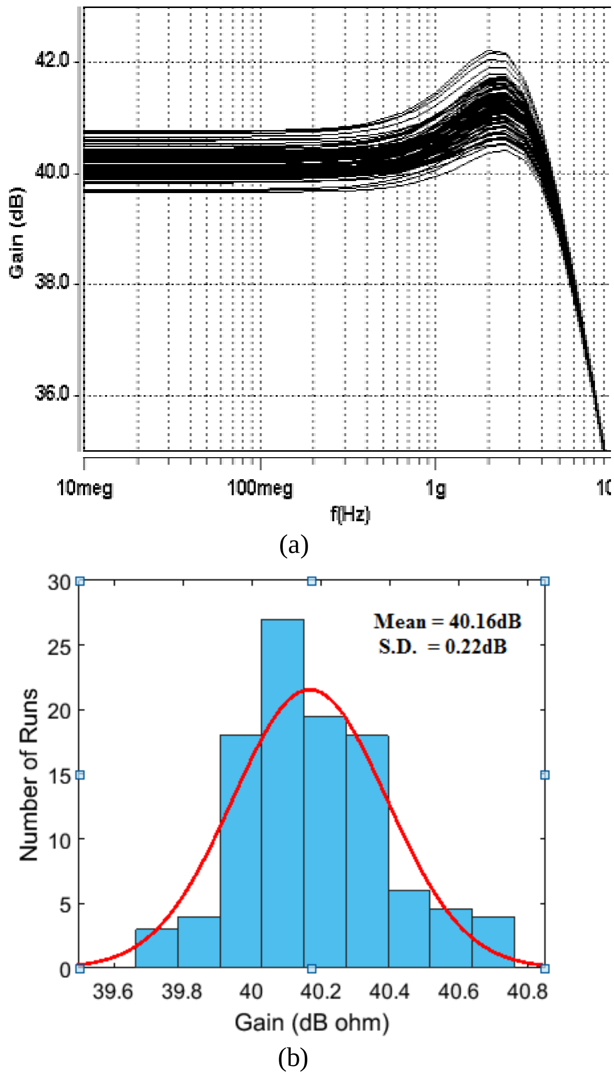


Fig. 12. Monte-Carlo for 100runs over (a) frequency response and (b) gain

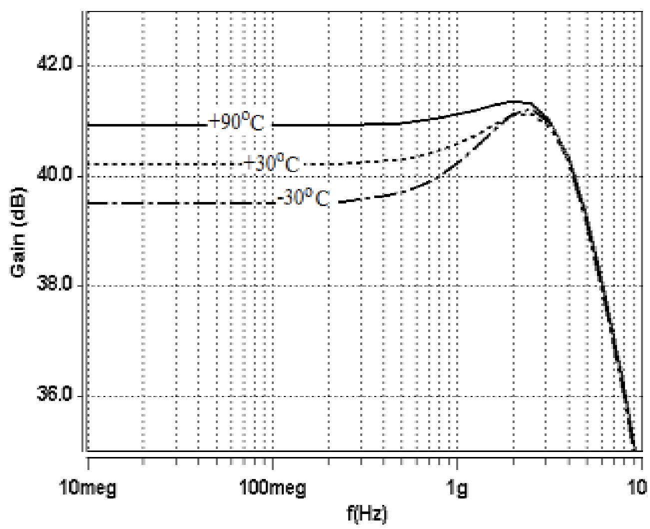


Fig. 13. Effect of temperature over frequency response

Table I. Numerically analysing the effect of temperature.

	-30ºC	+30ºC	90ºC
Gain (dBΩ)	39.49	40.19	40.90
Bandwidth (GHz)	7.6	6.88	6.24
Peaking (dB)	1.8	1	0.4

Table II. Numerically analysing the effect of supply voltage

	$0.9V_{DD}$	V_{DD}	$1.1\ V_{DD}$
Gain	40.13dBΩ	40.10dBΩ	40.06dBΩ
Bandwidth	7.8GHz	6.92GHz	6.8GHz
Power Consumption	1.4mW	1.9mW	2.5mW
Peaking	1.1dB	0.4dB	No peaking

Table III. Numerically analysing the effect of width variation of M_1 over the open-loop input resistance

	200 nm	400 nm	600 nm	800 nm	1 µm	1.5 µm	2 µm
R_{in} (Ω)	5339	2744	1670	1277	1044	731	565

Table IV. Analyzing the feedback network on input referred noise of the current-based TIA

	Open Loop TIA	Closed Loop TIA
Input Referred Noise Current	2.67µA@7.94GHz (30pA/√Hz)	2.35µA@7.94GHz (24pA/√Hz)

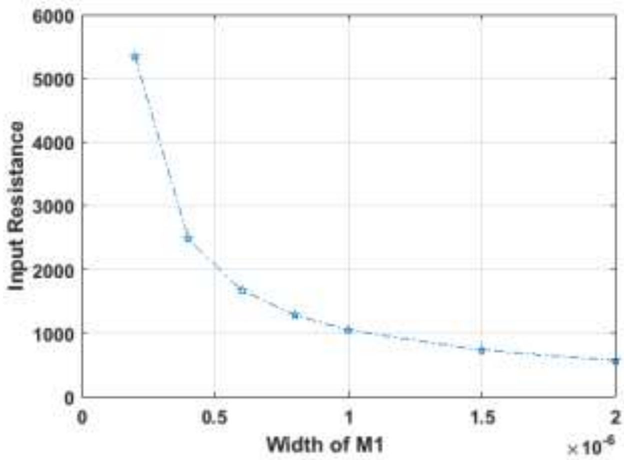


Fig. 14. Graphically analysing the effect of width variations of M_1 over the open-loop input resistance

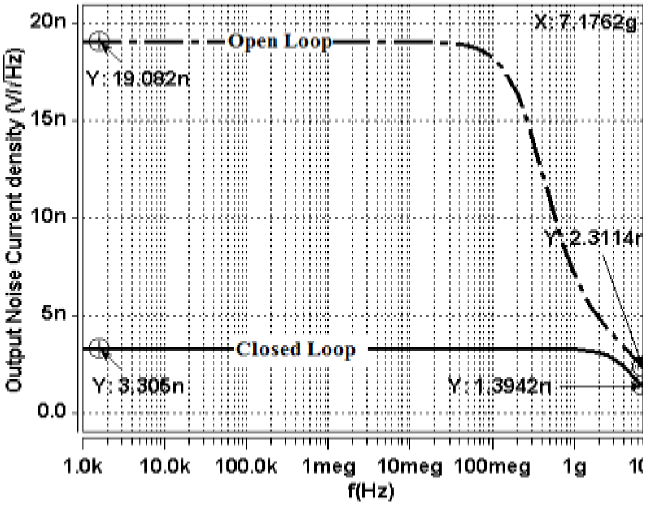


Fig. 15. Output Noise of the TIA stage

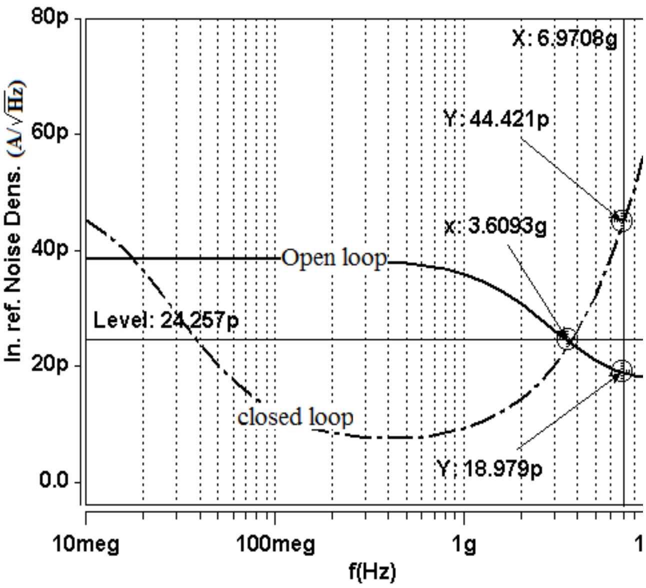


Fig. 16. Analysing the input-referred-noise of the current-based TIA with/without the feedback network

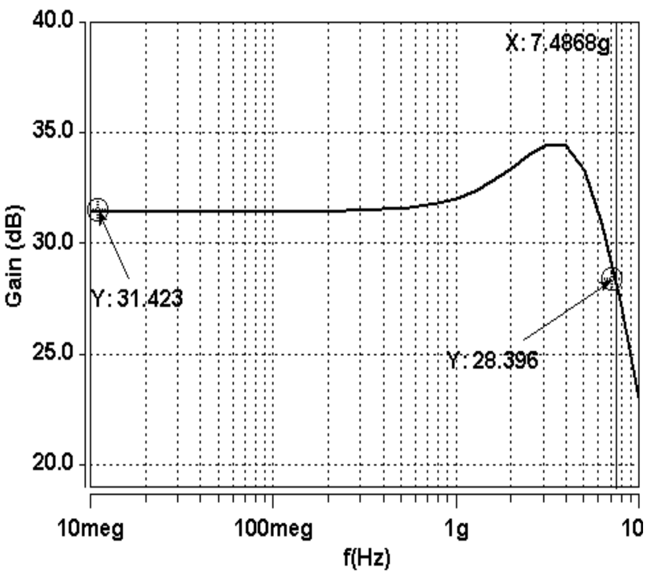


Fig. 17. Frequency Response of the Post Amplifier

Furthermore, the structure of the limiting amplifier stage is simulated using the same CMOS technology. A four-stage differential structure is used as the post amplifier, as discussed before. Figure (17) demonstrates the frequency response of the post amplifier. As it shown in figure (17), the LA stages provide 7.47GHz frequency bandwidth, 31.4dB gain and dissipate about 4.7mW power using 1.3 volt supply. Also, it is worth mentioning that the created peak over the frequency response will be decreased after connecting LA stages to the TIA stage.

5. The Complete Receiver System

The complete building block of the optical receiver system is demonstrated in figure (18). As in this figure, two TIA stages are used, where the second one is connected to a capacitance equal to the photodiode's capacitance. Hence, the TIA stage, which is connected to the photodiode, is supposed to amplify the main signal plus the noise, and the other one, named as replica TIA in the figure, is supposed to amplify the noise only. In such a way, the thermal noise of the circuit, which is uncorrelated and hard to predict, can be lessened in differential LA stages, as the common mode.

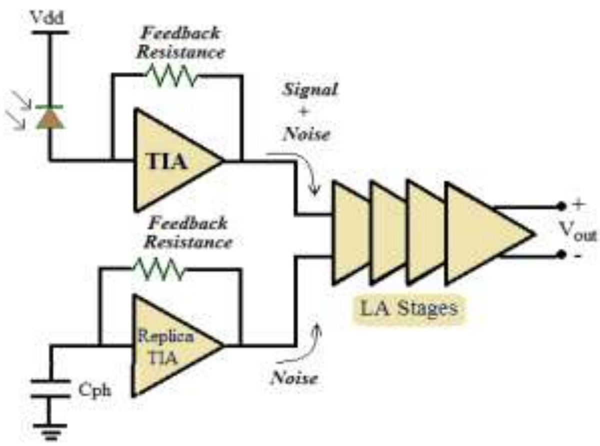


Fig. 18. Block Diagram of the Complete Optical Receiver

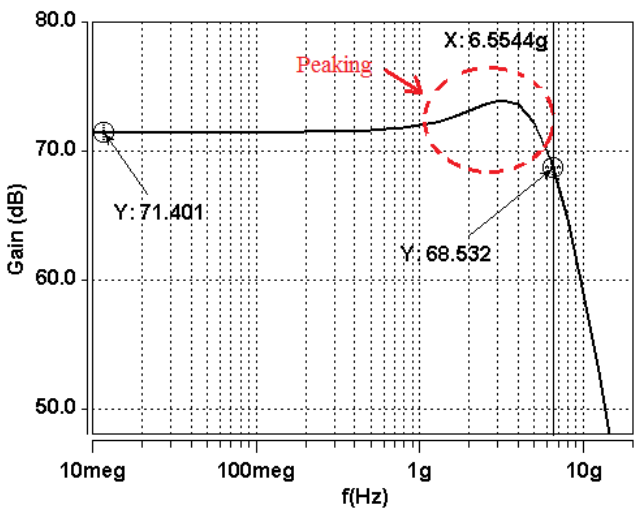


Fig. 19. Frequency Response of the Optical Receiver System

Additionally, four stages of the LA cell gains are used to obtain proper value of gain. The cell gains are cascaded, and the output signal is proposed to be properly amplified to provide proper domain and swing, in order to enter the digital circuitry.

Figure (19) demonstrates the frequency response of the complete system, shown in figure (18). As shown in this figure, the -3dB frequency of the whole system is equal to 6.55GHz, and the gain value is equal to 71.4dbΩ (3715Ω). Moreover, the complete system (consists of two stages of TIAs and four stages of LAs) dissipates only 7.7mW power, which is a low value.

Furthermore, the post layout simulations are done for the proposed TIA, to verify its performance at high-frequencies and examine the parasitic effects of the circuit on its behaviour. Figure (20) and figure (21) show the layout and post-layout simulations of the proposed TIA over the frequency response, respectively. The circuit occupies 84µm^2 area and the results show that the parasitic effects do not change the performance of the proposed TIA, dramatically, as shown in figure (21). The parasitic effects start to deteriorate the frequency response for higher than 20GHz applications, which is not inside the operating frequency of the proposed amplifier.

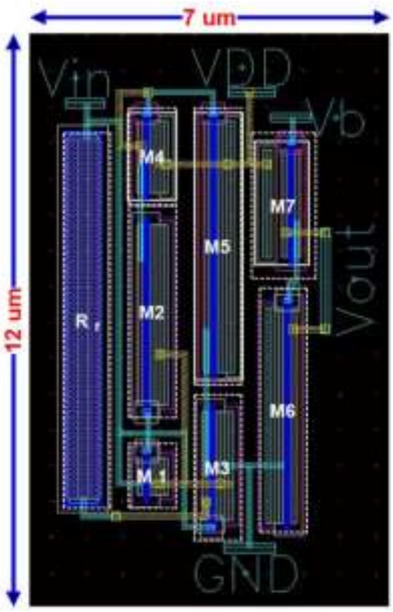


Fig. 20. Layout of the proposed TIA

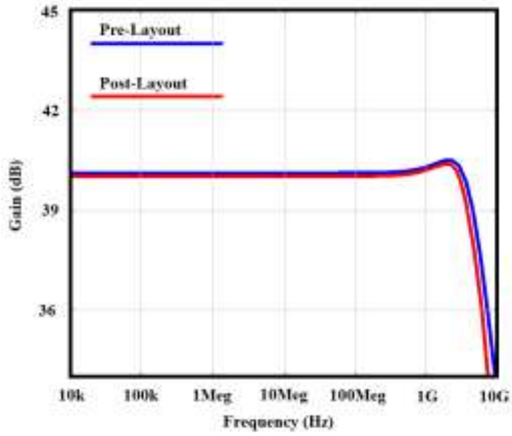


Fig. 21. Post-layout simulation of the frequency response

Table (5), briefly compares the parameters of the presented TIA circuitry with some of the references. It must be notice that the main objective of this manuscript is to reduce the power dissipation. Having table (5), the power dissipation of the presented transimpedance amplifier is significantly less than other references. However, comparing one parameter may not provide us a comprehensive comparison. So, two Figures of Merits (FOMs) are defined as follows, while their values are reported in table (5). The proposed design in this paper expresses a comprehensive superiority over most of the references, in terms of these definitions.

$$FOM1 = \frac{Gain \times B.W.}{P_{DC}} \left(\frac{\Omega.GHz}{mW}\right) \tag{30}$$

$$FOM2 = \frac{Gain \times B.W. \times C_{in}}{P_{DC} \times In.Ref.Noise} \left(\frac{\Omega \times GHz \times pF}{mW \times (pA/\sqrt{Hz})}\right) \tag{31}$$

6. Conclusions

In this manuscript, an active feed-forward, 10Gb/s, low-power optical communication receiver system is proposed. The TIA structure is based on topology of current-mirror structures, employing a voltage-current feedback to extend the -3dB frequency, and the LA structure is based on an improved topology of differential structures, which provides extra gain, while operates at high frequencies. In order to decrease the power dissipation, active inductors are used to resonate with the output capacitance of the TIA stage as well as LA cell gains; hence the bit rate is improved dissipating reduced power. Simulation results using 90nm CMOS technology for the TIA stage show 6.92GHz bandwidth, 40.1dBΩ transimpedance gain and 1.5mW power dissipation, while, for the whole receiver system the results show 6.55GHz frequency bandwidth, 71.4dBΩ gain and only 7.7mW power dissipation. Results and analysis verifies the proper performance of the presented circuit.

Table V. A comparison among the proposed transimpedance amplifier and other designs

	[22]	[23]	[24]	[25]	[26]	[27]	[28]	[29]	[30]	This Work
Year	2016	2013	2015	2016	2016	2011	2017	2017	2016	2018
Process (CMOS)	0.18µm	0.18µm	0.13µm	0.13µm	0.13µm SiGe BiCMOS	0.35µm	0.18µm	0.13µm SiGe BiCMOS	0.18µm	90nm
Gain (dBΩ)	58	46	50.1	54	72	54.2	59	83.7	55-69	40.1
Bandwidth (GHz)	8.1	8	7	11.5	38.4	2.3	7.9	32.1	1	6.92
Power Dissipation (W)	34.8m	31.5m	7.5m	45m	261m	58m	18m	150m	6m	1.5m
C_{pd} (fF)	300	250	250	-	-	500	300	-	-	200
Supply Voltage (V)	1.8	1.8	1.5	1.5	3.3	3.3	1.8	3.3	1.8	1
Input referred noise (pA/√Hz)	15	40	31.3	6.8	14.8	18.8	23	-	9.33	24
# passive inductors	2	2	0	2	0	0	2	0	0	0
FoM1	184.8	50.6	299	128	585	20	425	3276	417	466
FoM2	3.69	0.31	2.4	-	-	0.53	5.54	-	-	3.88

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